Analysis of Switching Effects in DC-DC Converters via Bias Point Computation

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Abstract—The paper describes a method for finding steady states in switched DC-DC converters, which is based on the SPICE bias point computation rather than a time-consuming transient analysis. The switched converter is modeled by unified substitutive circuits whose DC analysis determines directly the limit values of steady-state circuit variables at time instants when switches change their states. From these values one can derive e.g. the output voltage ripple or restore completely the steady-state signals.

I. INTRODUCTION

Fast transient analysis as well as DC and small-signal AC analyses of DC-DC converters can be performed by virtue of methods based on the averaging of circuit variables. The statespace averaging [1], [2], [3] belongs to the basic averaging approaches. However, its utilization is insignificant due to its problematic implementation in the SPICE-family analysis programs. A good implementation is offered by the alternative method of averaged modeling of the PWM switches in DC-DC converters, when the active and the passive switches are modeled by a pair of controlled current and voltage sources [4] or by other equivalent behavioral model [5], [6].

A drawback of all the averaging-based methods consists in the fact that the information about the switching phenomena is not present in the analysis results. That is why we cannot, for example, find out the output voltage ripple from the averaging analyses. Such features, which are connected to switch actions, can be revealed by means of the transient analysis on the switch-level model of the DC-DC converter. This analysis is considerably more time consuming than the transient analysis of averaged model. In addition, the analysis run must be sufficiently long in order to reach the steady state, since the SPICE-compatible programs do not have any internal algorithms for finding automatically the steady state. For circuits with rather long transitions to the steady state, the analysis must be repeated several times with the initial conditions, which are given by the circuit final state in the previous analysis run. The SPICE-compatible programs normally do not enable automating such activities. The run-toViera Biolkova and Zdenek Kolka Dept. of Radioelectronics Brno Univ. of Technology Brno, Czech Republic Email: {biolkova, kolka}@feec.vutbr.cz

run data sharing is possible only via writing the circuit final state into a file, followed by manual editing of this file, and the subsequent analysis run with reading the initial conditions from the above file. The analysis of switching phenomena becomes labored, time-expensive, and uneconomical, especially if the user is trying to establish the influence of circuit parameters, let us say the ESR of the filtering capacitor, on the output voltage ripple, because for such cases one must repeat the steady-state analysis more times.

A fundamentally different method of simulating the steady-state switching processes is described below. This approach uses the basic DC analysis in SPICE, i.e. the bias point computation. Thus, the time-consuming transient analysis is avoided. The method described below provides correct results on the assumption that time derivatives of circuit state variables, i.e. derivatives of capacitor voltages and inductor currents, vary linearly in time within each switching phase. This assumption is approximately fulfilled in most DC-DC converters, which are designed to work in the continuous conducting mode (CCM). Then the deflections of real waveforms from these piecewise linear curves are usually insignificant, causing negligible computational errors. As shown in the Conclusion, the above results can be used for a fast steady-state transient analysis.

II. DEMONSTRATION OF SWITCHING PROCESSES IN BOOST CONVERTER

The boost DC-DC converter in Fig. 1 has values of component parameters, designed for the CCM, including ESRs of the coil and the filtering capacitor. Results of the steady-state analysis from Micro-Cap 9 were obtained for the switching frequency $f_S = 100$ kHz and for duty ratio d = 0.25. The active (S) and passive (D) switches were modeled with the infinite off-resistance, with the on-resistance of the active switch $R_A = 10$ m Ω , and with the differential on-resistance of diode $R_D = 50$ m Ω . For simplicity, the threshold voltage of diode was not considered during the modeling. Resulting steady-state waveforms are shown in Fig. 2.

It is obvious from the case of $R_{out} = 6\Omega$ in Fig. 2 (a) that the waveforms of the state variables $v_C(t)$ and $i_L(t)$ can be approximated by a piece-wise curve in the frame of each switching phase. This is possible due to the relatively large time constants in the circuit in relation to the switching period. The waveforms of the time derivatives of state variables, i.e.



Figure 1. The boost DC-DC converter.



Figure 2. The steady-state voltages and currents in DC-DC converter from Fig. 1 for R_{out} (a) 6Ω , (b) 60Ω .

the capacitor current and inductor voltage, enable examining the measure of deflection of waveforms $v_C(t)$ and $i_L(t)$ from the piece-wise approximation. Within the phase of the active switch being in off-state, a linear drop of the capacitor current and a small increase in the inductor voltage are visible, as well as a small voltage drop on the inductor when the active switch is on. A piece-wise approximation of the waveforms $v_L(t)$ and $i_C(t)$ instead of the above approximation of state variable waveforms brings now more precise results: The state variables, obtained from the waveforms via integration, are now approximated by more precise parabolic curves instead of lines.

The waveforms of the output voltages in Fig. 2 show the influence of a rather large ESR of the filtering capacitor on the character of voltage ripple.

When increasing the load resistance 10 times (see Fig. b), a deformation of the curve of capacitor voltage appears, caused by the capacitor current drop during the off-state of the active switch, which is now considerably faster than in Fig. 2 (a). However, it is obvious that this phenomenon is well described by a parabolic function. This fact results from the capacitor current which is practically linearly falling with time.

When modeling the passive switch as bi-directional, to avoid the discontinuous current mode, and decreasing the filtering features of the converter by decreasing the values of C and L, we can observe a very good linearity of the derivatives of state variables also in the case of improperly small and atypical time constants of the circuit. Then the steady-state analysis, based on the above assumption, leads to results with acceptable error for a large scale of component values of the converter.

III. DC EQUIVALENTS OF CAPACITOR AND INDUCTOR IN THE CONVERTER STEADY-STATE

Consider the piece-wise waveforms of capacitor currents and inductor voltages according to Fig. 3. The switching period T_s is divided into switching phases 1 and 2 of lengths dT_s and $d'T_s$, which correspond to the on and off states of the active switch. Let us denote the points on the curve, matched with the right-side and left-side limits at time instants when switching phases 1 or 2 are finished, by symbols 1+ and 1-, or 2+ and 2-, respectively. The corresponding limits will be denoted I_{C1+} , I_{C1-} , etc.

The following equalities are true for capacitor voltages and inductor currents at time instants at the ends of phases 1 and 2:



Figure 3. Piece-wise approximation of time derivatives of converter state variables.

$$V_{C1-} = V_{C2+} + \frac{1}{C} \int_{0}^{dT_{s}} \{I_{C2+} + \frac{I_{C1-} - I_{C2+}}{dT_{s}}t\} dt, \qquad (1)$$

$$I_{L1-} = I_{L2+} + \frac{1}{L} \int_{0}^{dT_{s}} \{V_{L2+} + \frac{V_{L1-} - V_{L2+}}{dT_{s}} t\} dt, \qquad (2)$$

$$V_{C2-} = V_{C1+} + \frac{1}{C} \int_{0}^{d'T_{s}} \{I_{C1+} + \frac{I_{C2-} - I_{C1+}}{d'T_{s}}t\} dt, \qquad (3)$$

$$I_{L2-} = I_{L1+} + \frac{1}{L} \int_{0}^{d'T_{s}} \{V_{L1+} + \frac{V_{L2-} - V_{L1+}}{d'T_{s}}t\} dt$$
 (4)

Computing the integrals and a small arrangement yield

$$V_{C1-} = V_{C2+} + \frac{dT_s}{2C} (I_{C2+} + I_{C1-}),$$
 (5)

$$I_{L1-} = I_{L2+} + \frac{dT_s}{2L} (V_{L2+} + V_{L1-}), \qquad (6)$$

$$V_{C2-} = V_{C1+} + \frac{d'T_s}{2C} (I_{C1+} + I_{C2-}), \qquad (7)$$

$$I_{L2-} = I_{L1+} + \frac{d'T_s}{2L} \left(V_{L1+} + V_{L2-} \right).$$
(8)

Note that $V_{C1}=V_{C1+}$, $V_{C2}=V_{C2+}$, $I_{L1}=I_{L1+}$, $I_{L2}=I_{L2+}$ as a consequence of the continuity of the state-variable waveforms.

Eqs.(5) and (6) were generated as a solution of integrals (1) and (2) during the time interval of switching phase 1. That is why they represent a mathematical model of the capacitor and the inductor, respectively, during this switching phase. The corresponding model of the converter will include the onstate active switch, the off-state passive switch, the capacitor modeled by a controlled voltage source according to (5), and the inductor modeled by a controlled current source according to (6). Then the bias point computation will generate the limit values of circuit variables at point 1- (left-side limits).

Similarly, Eqs. (7) and (8) represent models of the capacitor and the inductor, respectively, during switching phase 2. An analysis of the corresponding model of the converter gives the limit values of circuit variables at point 2-.

However, also the right-side limits of circuit variables appear on the right sides of equations of controlled sources. Utilizing the continuity of state variables, we obtain them by an analysis of another two models of the converter. The model in phase 1, where the capacitor and the inductor are modeled by voltage and current controlled sources V_{C2-} and I_{L2-} , provides the solution at point 2+. The model in phase 2, excited by a voltage source V_{C1-} instead of capacitor and by a current source I_{L1-} instead of inductor, provides the solution at point 1+. Note that we analyze a model which is made up of four unified submodels instead of analyzing the original single model of the converter. The bias point computation will automatically provide the left- and right-side limits of every circuit variable at time instants when the switches change their states.

IV. DEMONSTRATION OF BOOST CONVERTER ANALYSIS

The auxiliary model of the boost converter from Fig. 1 for direct steady-state analysis via bias point computation is shown in Fig. 4. The inductor and the capacitor are modeled by controlled sources according to (5)-(8) in all four submodels. Both in the Micro-Cap 9 program and in the PSpice A/D program from OrCad 15.7, the analysis took only fractions of second, with identical results, summarized in Table I. The analysis was performed for $R_{out} = 60\Omega$, when a considerable "parabolic deformation" of curve $v_c(t)$ appears (see Fig. 2 b). The results obtained are in a good agreement with the steady-state analysis of switched model of DC-DC converter, which was obtained by laborious multiple transient



Figure 4. Auxiliary model of boost converter from Fig. 1 for direct steadystate computation.

PSpice circuit file for steady-state analysis of boost converter
.param C 1m L 6m Rout 60 RA 1 RD 1 Rc 1 RL 3 .param du 0.25 du2 {1-du} fs 10k
Vg in 0 60V
*phase 1- RL1- in x1- {RL} GL1- x1- sw1- value= +{ $V(in,x2+)/RL+(V(x2+,sw2+)+V(x1-,sw1-))*du/2/L/fs$ } EC1- out1- y1- value={ $V(out2+,y2+)+(I(EC2+)+$ + $I(EC1-))*du/2/C/fs$ } RA1- sw1- 0 {RA} RC1- y1- 0 {RC} Rout1- out1- 0 {Rout}
<pre>*phase 2- RL2- in x2- {RL} GL2- x2- sw2- value= +{V(in,x1+)/RL+(V(x1+,sw1+)+V(x2-,sw2-))*du2/2/L/fs} EC2- out2- y2- value= +{V(out1+,y1+)+(I(EC1+)+I(EC2-))*du2/2/C/fs} RD2- sw2- out2- {RD} RC2- y2- 0 {Rc} Rout2- out2- 0 {Rout}</pre>
<pre>*phase 1+ RL1+ in x1+ {RL} GL1+ x1+ sw1+ value={V(in,x1-)/RL} EC1+ out1+ y1+ value={V(out1-,y1-)} RD1+ sw1+ out1+ {RD} RC1+ y1+ 0 {Rc} Rout1+ out1+ 0 {Rout}</pre>
<pre>*phase 2+ RL2+ in x2+ {RL} GL2+ x2+ sw2+ value={V(in,x2-)/RL} EC2+ out2+ y2+ value={V(out2-,y2-)} RA2+ sw2+ 0 {RA} RC2+ y2+ 0 {Rc} Rout2+ out2+ 0 {Rout} end</pre>
.5114

analysis. In order to achieve the required precision, the time step upper limit of the transient analysis was set to $T_{max} = T_S$ /1e4 and in the final computation to $T_{max} = T_S$ /1e6. The maximum differences between the results compared are for the inductor current and the voltage V_{SW} (approx. 2.2%) at point 2+. For the remaining quantities they are considerably smaller.

V. CONCLUSIONS

A new method for finding immediately the coordinates of periodical steady-state of switched DC-DC converters via bias point computation is described. SPICE is solving here only the DC operating point of a special model of the converter, consisting of four dependent parts, in order to obtain directly the limit values of circuit variables at time instants of changing the states of switches. On the basis of these values, the converter parameters, associated with the switching effects, e.g. the output voltage ripple, can be found, as well as a complete reconstruction of all the signals in the periodical steady state can be performed without the necessity of timeconsuming transient analysis. Another possibility is to use the found limit values as initial conditions of final transient run with subsequent fast convergence to a steady state.

The method described is based on the assumption that the waveforms of time derivatives of state variables in the converter steady state are well matched to piece-wise functions with the border points at instants of switch transitions between their states. That is why it cannot be used for converters in the discontinuous current mode and for switched networks with abnormally low time constants.

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TABLE I. LIMIT VALUES OF CIRCUIT VARIABLES: PROPOSED METHOD (LEFT COLUMNS), TRANSIENT ANALYSIS (RIGHT COLUMNS)

$limit \rightarrow$	1-		1+		2-		2+	
$V_C[\mathbf{V}]$	79.811	79.807	79.811	79.807	79.817	79.813	79.817	79.813
$I_L[A]$	3.272	3.279	3.272	3.279	0.275	0.281	0.275	0.281
$I_C[\mathbf{A}]$	-1.328	-1.328	1.939	1.944	-1.054	-1.046	-1.328	-1.327
V_L [V]	59.902	59.902	-20.233	-20.231	-19.731	-19.728	59.992	59.992
$V_{SW}[V]$	32.723m	32.786m	80.168	80.165	79.726	79.723	2.813m	2.750m
V_{out} [V]	79.678	79.674	80.004	80.001	79.712	79.709	79.684	79.681