Symbolic Analysis Based on Graph Transformations

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Abstract— The paper deals with implementation details of a method for approximate symbolic analysis of linear circuits based on nontrivial transformations of voltage and current graphs. The method is based on eliminating the low-voltage branches from "high-voltage" loops and the low-current branches from "high-current" cuts. This goes beyond the simple edge deletion or contraction used in previous methods. The paper describes a graph transformation for decreasing the number of spanning trees and its computer implementation.

I. INTRODUCTION

An arbitrary network function in the frequency domain of lumped, linear and time-invariant circuits can be expressed symbolically as

$$F(s,\mathbf{p}) = \frac{s^m q_m(\mathbf{p}) + \dots + q_0(\mathbf{p})}{s^n r_n(\mathbf{p}) + \dots + r_0(\mathbf{p})}$$
(1)

where $\mathbf{p} = (p_1, p_2, ..., p_k)^T$ is a vector of the parameters of network elements (network parameters), *s* is the complex frequency, and $q_i(\mathbf{p})$, $r_i(\mathbf{p})$ are the sum-of-product expressions of network parameters. The complexity of (1) grows exponentially with circuit size [1].

It has been found that the majority of symbolic terms can be removed from large expressions without any significant numerical error [2]. This is the basic principle of all symbolic simplification methods, which are based on a combination of symbolic and numerical analyses. Usually, the approximated expression validity is checked numerically at several points $(f, \mathbf{p})_i$ in the frequency-parameter space.

The method described here belongs to the *Simplification Before Generation* (SBG) class where graphs or matrices representing the circuit are modified before the symbolic analysis in order to decrease the number of symbolic terms. A method, published as *Sifting Approach* [1], is based on a heuristic algorithm consisting in eliminating the device parameters from the numerator and the denominator submatrices separately. Another method [2], called *Two-graph Simplification*, deletes or contracts the edges of voltage and current graphs constructed for the numerator and the denominator separately.

We have proposed a different approach based on the twograph method. Instead of simply deleting or contracting the graph edges it modifies the graph structure in order to decrease the number of common spanning trees. Graphtheoretical proofs were published in [3]. This paper deals with an improved version exploiting the block decomposition of graphs.

II. MOTIVATING EXAMPLE

Let us consider a simple circuit in Fig. 1, whose network parameters are: $R_B = 36k\Omega$, $r_{\pi} = 4k\Omega$, $g_m = 35mS$, $R_L = 4k\Omega$.



Figure 1. Simple small-signal model.

The exact formula for the voltage transfer ratio is

$$K_{V} = \frac{v_{out}}{v_{in}} = -\frac{r_{\pi}}{R_{B} + r_{\pi}} g_{m} R_{L} .$$
 (2)

As $R_B >> r_{\pi}$, the formula can be further simplified. Let us limit ourselves to the SBG methods only. Resistor r_{π} cannot be simply removed or its terminal shorted. Both operations would cause an unacceptable error.

The circuit can be solved by the two-graph method [4]. The determinant of the nodal admittance matrix is

$$\det \mathbf{Y} = \sum_{t \in T(G_V) \cap T(G_I)} \varepsilon(t) Y^{(t)} , \qquad (3)$$

where $Y^{(t)}$ is the tree-admittance product of tree t, $T(G_V)$ and $T(G_I)$ are the sets of all spanning trees of voltage and current graphs. The intersection $T(G_V) \cap T(G_I)$ represents the common spanning trees of G_I and G_V . $\varepsilon(t) = \pm 1$ is the tree sign. The technique of augmented circuit [2] allows computing both the numerator and the denominator at the same time. Fig. 2 shows an example for voltage transfer.

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Figure 2. Augmented circuit for voltage transfer ratio.

The VCVS in Fig. 2 is represented by a suitable admittance model [5]. The determinant of the admittance matrix is

$$\Delta = \Delta_1 + A \Delta_2 \text{ , and} \tag{4}$$

$$K_V = \frac{\Delta_2}{\Delta_1} \quad . \tag{5}$$

Since A is a symbol, the terms belonging to Δ_1 or Δ_2 are easy to recognize.

Fig. 3a shows voltage and current graphs for the augmented circuit. Edges "1" and "A" model the VCVS [5].



Figure 3. a) Original and b) modified graphs.

Let the voltage across input edge "1" be 1V. Then the voltage across r_{π} is 0.1V. The voltage can be neglected in loops $1-G_B$ - g_{π} and $1-G_B$ - g_m but not in loop g_{π} - g_m . A simple modification in Fig. 3b removes g_m and g_{π} from the "high-voltage" loops only. The simplified formula for the voltage transfer ratio obtained using (4) and (5) is then

$$K_{V}' = -\frac{r_{\pi}}{R_{B}}g_{m}R_{L}$$
 (6)

An inspection of the voltage and current graphs from Fig. 3b shows that they represent a CCCS instead of r_{π} and VCCS.

This simple example shows the basic principle of the proposed method – selective removal of the low-voltage edges from the "high-voltage" loops. Similar transformations can be found for cuts of the current graph. The method will be called topological simplification (TSBG).

III. TOPOLOGICAL SBG

A. Graph Transformations

Let G be a graph. Then V(G) is a set of its vertices, E(G) is a set of its edges, and T(G) is a set of its trees. The incidence of edge e in graph G, $\rho(e,G) = (i, j)$, assigns two

vertices i, j to edge e. An edge with the incidence (v,v) is called selfloop. Graph G is said to be separable if there is a vertex whose removal splits the graph into two or more components. A block is a maximal nonseparable subgraph.

The basic operation of TSBG is the separation of a connected subgraph [3].

Definition 1: Separation of a connected subgraph G_s from a graph G is an operation that transforms G into

$$G' = \widetilde{G} \cup G_8 \quad , \tag{7}$$

where \widetilde{G} is a subgraph whose edge set is $E(\widetilde{G}) = E(G \setminus G_S)$. The incidence $\rho(e,G) = (v_i, v_j)$ of any edge $e \in E(\widetilde{G})$ is transformed into $\rho(e,\widetilde{G}) = (f(v_i), f(v_j))$, where *f* is

$$f(v) = \begin{cases} v_{\rm c} & \text{if } v \in V(G_{\rm S}) \\ v & \text{otherwise} \end{cases}$$
(8)

 v_c is an arbitrary but fixed vertex $v_c \in V(G \setminus G_S) \cap V(G_S)$. The operations will be denoted as follows:

$$\widetilde{G} = G \Longrightarrow G_{\mathrm{S}}, \qquad G' = G \triangleright G_{\mathrm{S}}.$$
 (9a,b)



a) original graph G; b) graph $\widetilde{G} = G \Longrightarrow G_{\rm S}$; c) $G' = G \triangleright G_{\rm S}$.

Fig. 4 demonstrates the separation of $G_S = \{e_1, e_2, e_3\}$. The transformation does not change the number of edges and vertices and decreases the number of spanning trees of *G*'. Proof can be found in [3].

B. Loop and Cut Transformations

Let the circuit be represented by the current graph G_{I} and the voltage graph G_{V} with edges $e_1, e_2, ..., e_b$, whose weights are the magnitudes of branch currents and voltages for a particular frequency.

Let $L_1, L_2, ..., L_B \subseteq G_V$ be all the loops of the voltage graph G_V . The voltage $v(e_j)$ of an edge $e_j \in E(L_i)$ will be considered numerically negligible in loop L_i if

$$\left| v(e_j) \right| < \varepsilon_{\mathrm{V}} \max_{h \in E(L_i)} |v(h)| \quad , \tag{10}$$

where $\varepsilon_{V} \in (0, 1)$ is the threshold value. Such an edge is a candidate for being removed from L_{i} .

Let us assume that the voltage graph G_V can be decomposed into two edge-disjoint subgraphs G_V^H and G_V^L and the condition

$$\max_{e \in G_{V}^{L} \cap L} |v(e)| < \varepsilon_{V} \max_{e \in L} |v(e)| \quad , \tag{11}$$

holds for any loop $L \subseteq G_V$ that is contained in both subgraphs. Then it is possible to remove the low-voltage edges of G_V^L from high-voltage loops by the separation

$$G'_{\rm V} = G_{\rm V} \triangleright G_{\rm V}^{\rm L} \ . \tag{12}$$

In the example from Section 2, $G_V^L = \{g_\pi, g_m\}$. The separation of a disconnected subgraph is performed component-by-component.



Subgraph separation (12) can be divided into *elementary* operations exploiting the block structure of both G_V^L and \widetilde{G}_V . Condition (10) has been formulated for loops contained in both subgraphs. Let us assume that G_V^L is separable with blocks B_i^V . As there is no loop contained in two or more blocks, the separation of any block B_i^V , which is considered the *elementary operation*, satisfies (10) as well. Graph $\widetilde{G}_V = G_V \Rightarrow G_V^L$ may also be separable. The loops contained in \widetilde{G}_V form disjoint subsets. It is easy to augment G_V^L such that the resulting graph \widetilde{G}_V becomes nonseparable.

Fig. 5b shows the separation of subgraph $G_S = \{e_1, e_2, e_3, e_7, e_8, e_9\}$ having two blocks $(B_1 = \{e_1, e_2, e_3\}$ and $B_2 = \{e_7, e_8, e_9\}$ that can be separated independently, Fig. 5c,d. \widetilde{G} consists of two blocks $(\widetilde{B}_1 = \{e_4, e_5, e_6\}, \widetilde{B}_2 = \{e_{10}, e_{11}, e_{12}\})$. Augmenting G_S by the complement of \widetilde{B}_1 or \widetilde{B}_2 results in nonseparable \widetilde{G}' , Fig. 5e,f.

It can be also shown that removing small-current branches from high-current cuts leads to decomposing $G_{\rm I}$ with respect to a threshold value $\varepsilon_{\rm I} \in (0, 1)$ into two edgedisjoint subgraphs $G_{\rm I}^{\rm H}$ and $G_{\rm I}^{\rm L}$ [3]. If for any loop $L \subseteq G_{\rm I}$ contained in both subgraphs the condition

$$\min_{e \in E(L)} |i(e)| < \varepsilon_{\mathrm{I}} \min_{e \in E(G_{\mathrm{I}}^{\mathrm{H}} \cap L)} |i(e)|$$
(13)

holds then it is possible to perform the separation

$$G'_{\mathrm{I}} = G_{\mathrm{I}} \triangleright G_{\mathrm{I}}^{\mathrm{H}} \quad . \tag{14}$$

C. Relation to classical methods

Let us consider the separation of an edge e_c with admittance parameter y_c from a graph G, Fig. 6b.

$$G' = G \triangleright \{e_{c}\} \quad . \tag{15}$$

All the spanning trees of G' contain the edge e_c . Thus all numerator and denominator terms contain y_c , which can be evidently reduced. The separation is equivalent to $y_c \rightarrow \infty$.



Figure 6. a) Graph G; b) $G'=G \triangleright \{e_{c}\}$; c) $G''=G \triangleright \{\overline{e}_{c}\}$.

The separation of complement $\overline{e_c} = G \setminus e_c$ of edge e_c

$$G'' = G \triangleright \{\overline{e_{c}}\}$$
(16)

always forms a self-loop in G''. No tree can contain y_c . The separation is equivalent to $y_c \rightarrow 0$. Thus the methods of [1] and [2] are just special cases of a more general TSBG.

IV. ALGORITHMS

The error-control strategy is similar to the method of [6]. Assuming m reference points the error criterion is

$$\varepsilon_A = \max_{i=1..m} \frac{20\log|E(\omega_i)|}{\Delta M_{\omega_i}} + \frac{\arg(E(\omega_i))}{\Delta \varphi_{\omega_i}} , \qquad (17)$$

where $E(\omega) = F_A(\omega) / F_R(\omega)$ and ΔM_{ω_i} , $\Delta \varphi_{\omega_i}$ are inverse weights. $F_A(\omega)$ and $F_R(\omega)$ are approximated and reference network functions, respectively.

compute reference numerical solution; while $\varepsilon_A < \varepsilon_{max}$ { generate all possible operations; compute the error of each operation; perform operation(s) with the lowest error; update numerical solution and ε_A ; }

undo last operation;

Figure 7. Main cycle of simplification method.

The simplification algorithm is applied twice. First, it performs the parametric simplification, i.e. the elementary operations are $p_i \rightarrow 0$ and $p_i \rightarrow \infty$ for each parameter. The method of large-change sensitivity [7] is used for error computation. This step substantially decreases the circuit size. The cost is approximately $O(r m n^3)$, where *n* is the circuit matrix order, *r* is the number of removed parameters, and *m* is the number of reference points.

find a spanning tree with the lowest voltage-magn. product; sort chords c_i in ascending order; $S_A = \emptyset; S_S = \emptyset;$ for i = 1...(b-n+1) { generate basic loop L_i for chord c_i ; $S_B = \{S_{A,j} | S_{A,j} \cap L_i \neq \emptyset\};$ if S_B is empty { add L_i to $S_A;$ } else { $U = \left(\bigcup_i S_{B,i} \right) \cup L_i;$

remove members of $S_{\rm B}$ from $S_{\rm A}$; add U to $S_{\rm A}$; for all j if $\max_{e \in S_{{\rm B},j}} |v(e)| < \varepsilon_{\rm V} \max_{e \in L_i} |v(e)|$, add $S_{{\rm B},j}$ to $S_{\rm S}$; }

}

Figure 8. Generation of elementary operations for $G_{\rm V}$.

The next step consists in separating the subgraphs (or their blocks) that fulfill (11) or (13), Fig. 8. Let the graph $(G_V \text{ or } G_I)$ be connected and have *n* vertices and *b* edges. Any spanning tree *t* consists of exactly *n*-1 edges - *twigs*. The remaining edges will be called *chords* [7]. A *basic loop* is formed from one chord and some twigs. Let S_A and S_B be auxiliary sets of subgraphs and S_S a set of candidates for separation. The symbol $S_{A,i}$ represents the *i*-th member of S_A . The algorithm for the current graph is similar. Candidates are generated for all frequency samples. The cost is approximately $O(m (n^3+b))$.

V. EXAMPLE ANALYSIS

The method is demonstrated on an analysis of a currentfeedback amplifier in Matlab. Parametric preprocessing reduced the original 100 network parameters to 14. The topological algorithm separated two subgraphs from the voltage graph and one subgraph from the current graph. The formula for voltage transfer was further simplified by means of the SAG method [6].

TABLE I. RESULTS OF SIMPLIFICATION STEPS

accuracy		parametric	graph-based	SAG
$\Delta M_{\rm max}$	allowed	± 1 dB @ 1kHz and 600kHz		
	actual	0.47dB@1kHz	0.56dB@600kH	0.21dB@1kHz
$\Delta \varphi_{\rm max}$	allowed	± 3° @ 1kHz and 600kHz		
	actual	2.4°@600kHz	2.4°@600kHz	3.0°@600kHz
# of numer. terms		44	4	3
# of denom. terms		232	65	46
# of parameters		14	14	14
runtime		4.9s	1.3s	0.9s



Figure 9. Current-feedback amplifier.

CONCLUSION

The method of topological simplification allows reaching a higher degree of simplification than the parameter-based SBG techniques do. The result is a simplified circuit model that is analyzed symbolically. An important property is that the graph transformation is based on physical relations in the circuit in contrast to the rather mathematical methods.

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