NOVEL SIGNAL FLOW GRAPHS OF CURRENT CONVEYORS

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ABSTRACT

Economical signal flow graphs (*SFG*) of current conveyors *CCII+* and *CCII-* are introduced in this contribution. Described method is based on the linear transformation of circuit equations with the aim to decrease their number. The evaluation of the *SFG* is then modest.

INTRODUCTION

Due to the growing role of current-mode analog signal processing, the current conveyors become important building blocks in many applications. Besides the current conveyors in the integrated circuit form, the principle of current conveyance is used in other building blocks as transimpedance OpAmps.

Thanks to the firm *LTP Electronics*, the integrated positive current conveyor *CCII01* is currently available [1]. As regards transimpedance OpAmps, the *Analog Device's* monolithic OpAmp *AD 844* with compensation pin is most popular in analog signal processing [2].

Nowadays, some novel high-frequency and low-sensitivity current conveyor-based circuits are developed [1-4]. However, the effective tool for the synthesis facilitation and fast control analysis is not available. The specially modified signal flow graphs can hold this function.

MODELING OF CURRENT CONVEYOR USING SFG

The well-known schematic and circuit representation of current conveyor is in Fig.1. The classical circuit equations are as follows:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} & & & V_Y \\ 1 & & & I_X \\ & \pm 1 & & V_Z \end{bmatrix}.$$

The sign +/- is true for the positive/negative current conveyor.

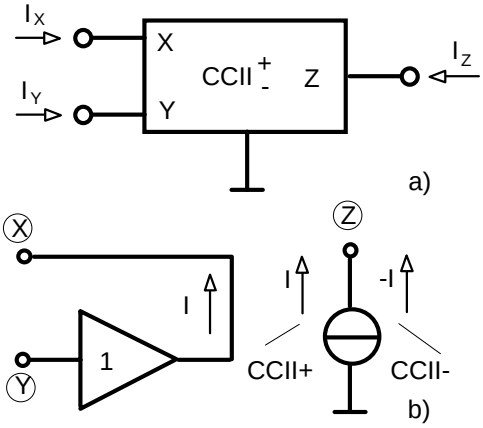


Fig.1. a) Black-box representation of the current conveyor, b) its circuit model.

However, these equations are not suitable for the generation of appropriate *SFG*. Better way is to utilize modified nodal approach (*MNA*).

Let us consider circuit in Fig.2 a). Following equations are true:

$$\begin{aligned} V_X &= V_Y \\ I_1 &= Y_1(V_1 - V_X) \\ I_2 &= Y_2(V_2 - V_Y) \\ I_Y &= Y_2(V_Y - V_2) \\ I_X &= Y_1(V_X - V_1) - I \\ I_Z &= Y_3(V_Z - V_3) \mp I = \\ &= Y_3(V_Z - V_3) \pm I_X \mp Y_1(V_Y - V_1). \end{aligned}$$

The graph representations of aforementioned equations are in Fig. 2b) and c). First *SFG* can be used if the current *I* needs to be calculated. Second one represents the reduced graph where the variable *I* is eliminated from circuit equations.

After generalization, the general rules of compiling *CCII* graphs are derived in Fig.3. In the reduced graph, the variables of node *X* are omitted. Admittances connected to this node create transmissions of branches to the output node *Z* and

are signed as minus or plus depending on the type of *CCII*.

The way how to handle that graphs will be explained in the set of examples. All circuit analyzed below are assumed of [3].

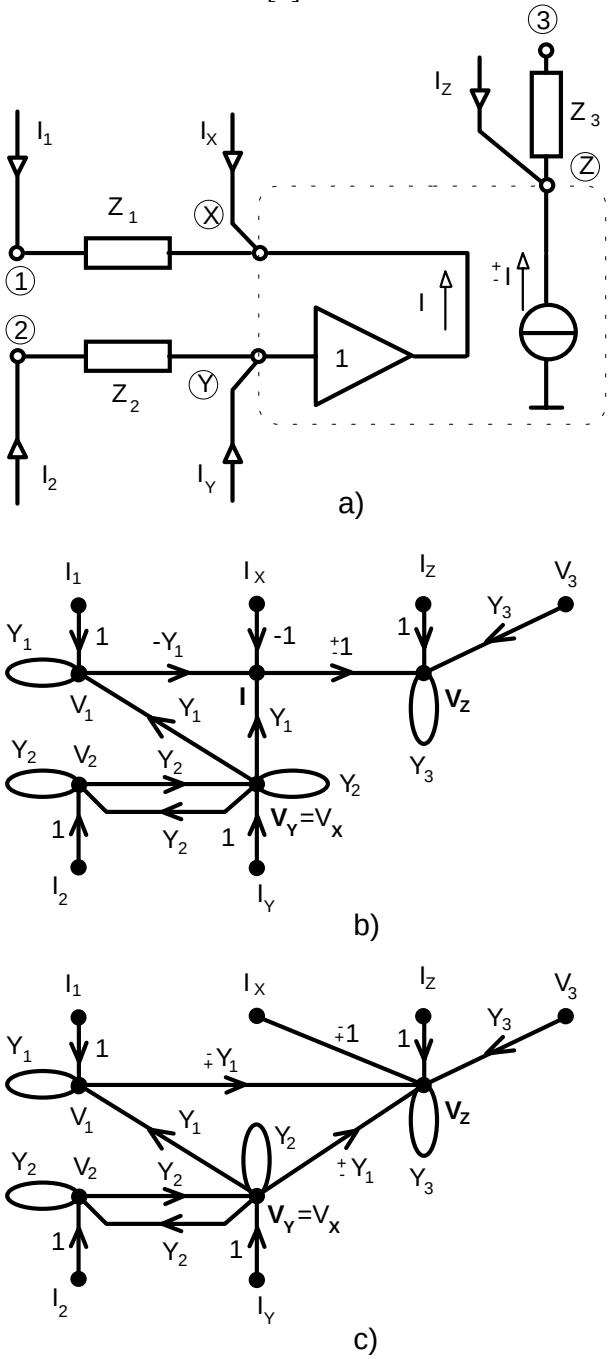


Fig.2. a) Example of circuit with *CCII*,
b) corresponding *SFG*, c) reduced *SFG*.

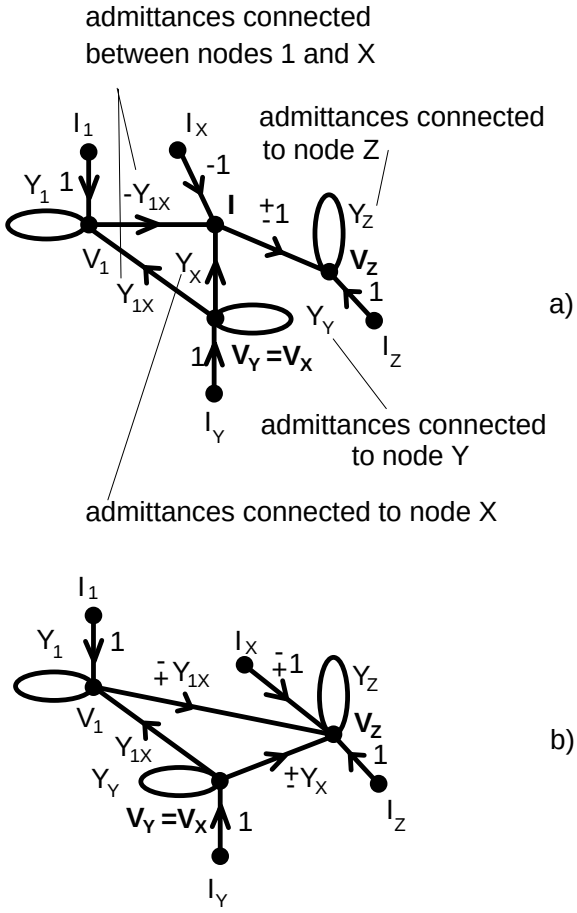


Fig.3. The principle of compilation of *CCII SFG* :
a) normal, b) reduced graph.

ILLUSTRATION EXAMPLES

Example No.1: *Current integrator*.

The current integrator operates so that the current I_z is the integral of input current I_y. In this case, it is convenient to use *SFG* comprising the conveyor current. The *SFG* in Fig.4b) has been compiled in accordance with the rule described above. In principle, this integrator operates independently of the load. In addition, we are not interested in the voltage V_z. That is why the dashed part of *SFG* in Fig.4b) is redundant.

Resulting graph is very simple and its evaluation leads to the conclusion

$$\frac{I_Z}{I_Y} = \frac{1}{sRC}.$$

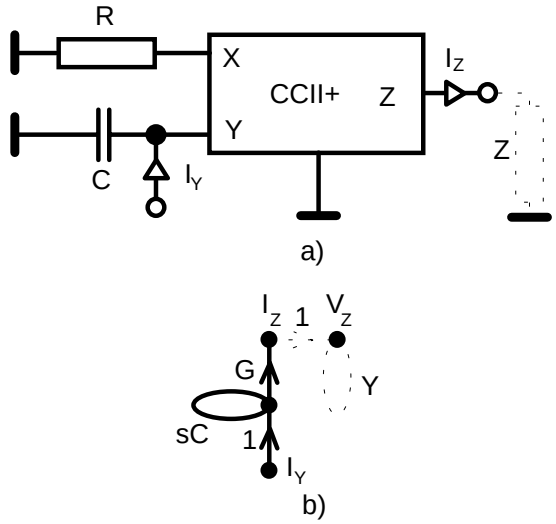


Fig.4. a) Current integrator, b) corresponding graph

Example No.2: *Gyrator*.

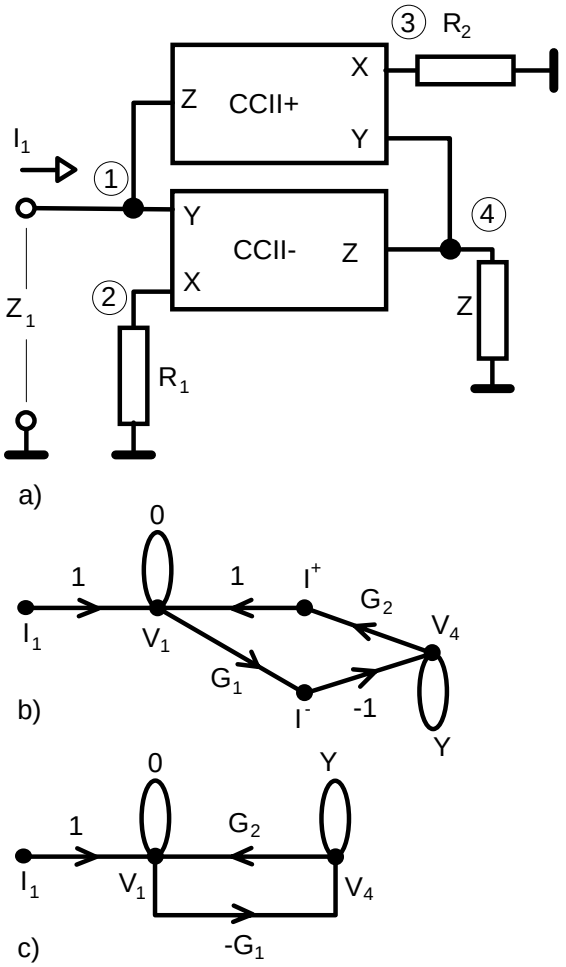


Fig.5. a) Gyrator with two current conveyors, b) *SFG*, c) reduced *SFG*.

Scheme of two-conveyor's gyrator is in Fig.5a) and corresponding *SFG*'s in Fig. b) and c). The self-loop with zero transfer has appeared in node V_1 because no admittances are connected to this node.

After graph evaluation, the equation for input impedance is obtained:

$$Z_1 = \frac{V_1}{I_1} = \frac{Y}{0-(-G_1G_2)} = \frac{R_1R_2}{Z}.$$

Example No.3: *Current mode filter*.

The corresponding graph in Fig. 6 b) or c) can be evaluated by classical way. The second order transfer function is obtained after short arrangement:

$$\frac{I_{out}}{I_{in}} = \frac{1}{s^2C_1C_2R_1R_2 + sC_1(R_1+R_2)+1}.$$

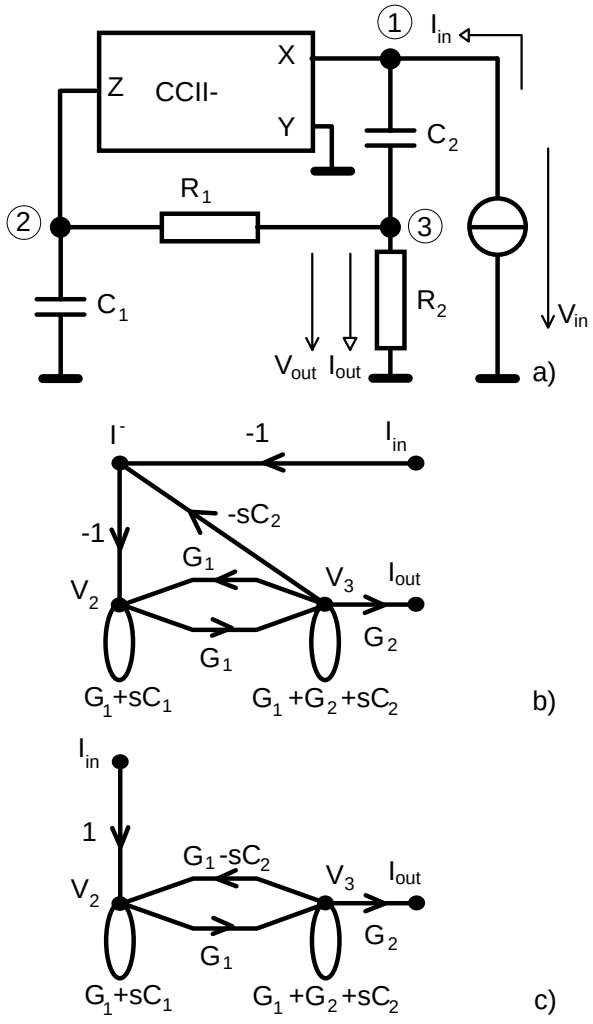
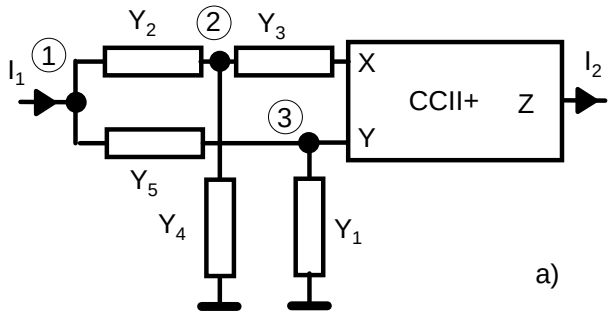


Fig.6. a) Second-order current filter, b) *SFG*, c) reduced *SFG*.

Example No.4: *General current mode biquad filter*.



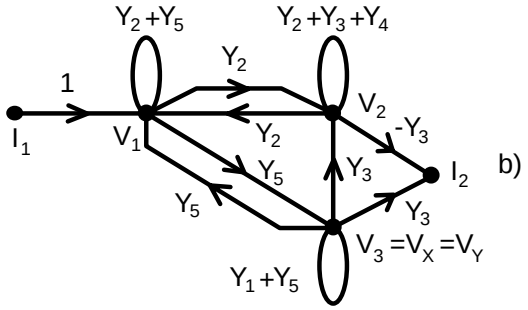


Fig.6. a) General current mode biquad filter, b) *SFG*

The resulting current-mode transfer function can be written after graph evaluation and short algebraical arrangement:

$$\frac{I_2}{I_1} = \frac{Y_3\left(Y_4Y_5 - Y_1Y_2\right)}{Y_1Y_5\left(Y_2+Y_3+Y_4\right)+Y_1Y_2\left(Y_3+Y_4\right)+Y_2Y_4Y_5}$$

CONCLUSION

This contribution proposes the principle of fast analysis of circuit comprised current conveyors using novel signal flow graphs. This method has been verified in systematic comparison with the outputs of program *COFACTOR* for the symbolic analysis of linear circuits [6], [7].

Acknowledgement

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