Nonlinear On-chip Capacitor Characterization

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***Abstract*—The paper deals with a modification of the CBCM method for nonlinear on-chip capacitance characterization. The proposed modification uses two DC swept sources to measure the whole nonlinear Q-v characteristic in both polarities without the necessity to switch the object being measured. A test-chip implementing the method was designed and manufactured in the 0.35µm CMOS process. It was used for MOSCAP characterization in the full operating voltage range.**

I. INTRODUCTION

The CBCM method (Charge-Based Capacitance Measurements) has found extensive use in on-chip capacitor measurements in the femtofarad range [1]. The method is characterized by high resolution although it is based on equipment found in any average laboratory. CBCM was originally developed for linear interconnect capacitance measurements. Sub-femtofarad resolution has been reported [2]. A charge injection error-free variant has been developed [4].

This paper shows a modification of the method to enable nonlinear capacitance characterization. A test-chip implementing the method was designed and manufactured in the 0.35µm CMOS process for on-chip MOSFET gate capacitance characterization.

II. STANDARD CBCM METHOD

Fig. 1 shows the principle of the classical version of CBCM [1]. The test structure consists of a pair of NMOS and PMOS transistors connected in a pseudo-inverter configuration, each of them having its own gate input. The pseudo-inverter structure on the left is used as reference to increase the resolution. The structure on the left is identical to the one on the right in every manner except that it does not include the target capacitance C_x to be characterized. The left and right structures are both driven by two non-overlapping signals. The purpose of these non-overlapping waveforms is to ensure that only one of the two transistors on either the left or the right side is conducting current at any given time. When the PMOS transistor turns on, it will draw charge Q from V_{dd} to charge up the target capacitance measured. This amount of charge will subsequently be discharged through the NMOS transistor into ground. An ammeter can be placed at the source of the PMOS (or, alternatively, at the source of the NMOS) to measure this charging current. The actual waveform of this charging current is not important - only its DC component needs to be measured [2]. The difference between the two DC current values is used to extract the measured target capacitance C_x as given by

$$I - I' = (Q - Q')\, f = V_{dd}\, C_x f \ , \qquad (1)$$

where $Q - Q' = V_{dd}\,((C_i + C_x) - C_i)$, f is the switching frequency, C_i is the parasitic capacitance and DC currents I and I' are introduced in Fig. 1.

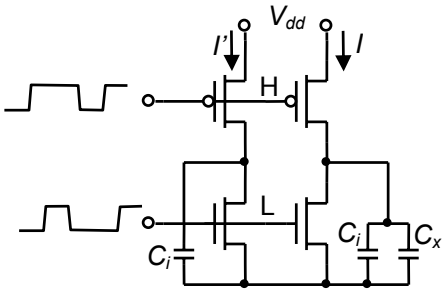

Figure 1. Classical version of CBCM method.

It is obvious from (1) that the currents and thus the resolution of the method can be increased by means of increasing V_{dd} and the frequency. V_{dd} is limited by the technology and the maximum frequency is determined by the on-resistance of switching transistors. The capacitance under test must be "completely" charged and discharged during one period. The switching transients can be speeded-up by increasing the switching transistor width, i.e. by decreasing their on-resistance. This can be done only in a limited range because the transistor enlargement increases the gate capacitances and thus increases the undesirable charge injection from driver circuitry to the device under test. Fig. 2 shows schematically the waveforms of switching transients valid for both the left and the right structures in the basic configuration from Fig. 1.

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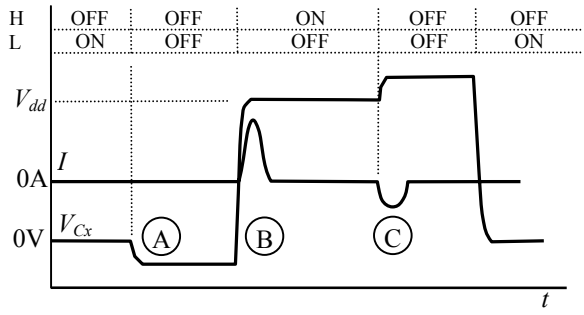


Figure 2. Switching transients (not to scale).

The undesirable charge injection takes effect both for both L and H switches. At the start of switching cycle, V_{Cx} is zero. Charge injection during switching off the L switch causes V_{Cx} to be negative. The total voltage swing of C_x is then greater than V_{dd}. Another parasitic injection occurs during switching off the H switch causing a spike on I or I'.

Let us consider a single pseudoinverter from Fig. 1 loaded by a capacitor C_L representing either C_i or C_x+C_i. The charge drawn from the V_{dd} source during one period is

$$Q_{dd}(C_L) = Q_A(C_L) + Q_B(C_L) + Q_C(C_L) \ , \qquad (2)$$

where Q_A, Q_B, and Q_C are the contributions for transients A through C, Fig. 2. Since Q_{dd} is a nonlinear function of C_L, the parasitics of the left and the right structures cannot compensate as in (1) even in the case of perfect matching

$$Q - Q' = Q_{dd}(C_x + C_i) - Q_{dd}(C_i) \neq V_{dd}\, C_x \ . \qquad (3)$$

This represents the systematic error of CBCM, which is both process and matching sensitive.

The approximate analysis of charge injection is based on a lumped switching model introduced in [6]. The lumped model is valid if the gate voltage drops much slower than the intrinsic carrier transmit time in the transistor ($\tau_C = R_{on} C_{ox} / 4$).

The transistor is characterized by the threshold voltage V_T, the current factor $\beta = \mu C'_{ox} W_{eff} / L_{eff}$ and by the overlap capacitances C_{GDO} and C_{GSO}.

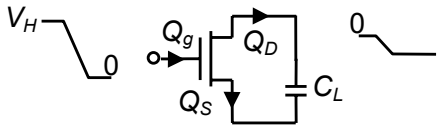


Figure 3. Model for transients A and C.

The undesirable charge injections A and C occur during the switching off process. For transient times much larger than τ_C, the channel charge is initially split equally between the source and the drain. The redistribution of charge from the drain to the source is determined by their voltage difference and time constants [7].

The initial capacitor voltage is zero. The capacitor voltage will be negative after the transient but small enough not to cause a significant current through the drain-bulk junction, Fig. 3. If the gate voltage is a ramp function which begins to fall at time 0 from the high value V_H toward 0 at a falling rate U, the charge injected into the drain terminal can be expressed in a closed form as [6]

$$Q_D(C_L) = -\sqrt{\frac{\pi U}{2\beta}} \frac{C_L C_{GD}}{\sqrt{C_L + C_{GD}}} \mathrm{erf}\left(\frac{(V_H - V_T)\sqrt{\beta}}{\sqrt{2U(C_L + C_{GD})}} \right) - C_{GDO} V_T \ , \qquad (4)$$

where $C_{GD} = C_{GDO} + C_{ox}/2$.

Using the charge-conservation principle, the charge injected into the source terminal will be

$$Q_S(C_L) = -(V_H - V_T) C_{ox} - (C_{GDO} + C_{GSO}) V_H - Q_D(C_L) \ . \qquad (5)$$

The parasitic charges from (2) will be

$$Q_A(C_L) = -Q_D^N(C_L) \ , \qquad (6a)$$

$$Q_C(C_L) = Q_S^P(C_L) \ , \qquad (6b)$$

where Q_D^N and Q_S^P are determined from (4) and (5) using the NMOS or PMOS transistor parameters.

Fig. 4 represents the equivalent circuit for transient B when H is switched on. The capacitor is charged from the initial voltage 0 to V_{dd} (the negative initial capacitor voltage has been counted in Q_A).

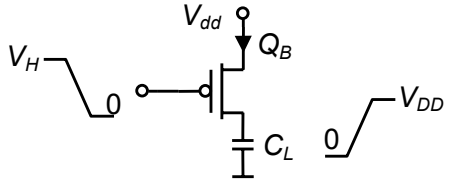


Figure 4. Equivalent circuit for transient B.

Using the charge-conservation principle, the charge drawn from the V_{dd} source will be simply

$$Q_B(C_L) = C_L V_{dd} + C_{GSO} V_H + C_{GDO}(V_H + V_{dd}) + C_{ox}(V_{dd} - V_T) \ . \qquad (7)$$

In the case of ideal matching Q_B can be compensated as it depends linearly on C_L.

III. Modified CBCM Method

The CBCM method is normally used to characterize linear capacitances. The simple version of the method is not well suited for the characterization of nonlinear capacitors such as MOSFET gate capacitances. Nonlinear capacitors are characterized by the C-v or Q-v curves. The standard CBCM allows V_{dd} sweeping but for low voltages the measured current decreases and the method resolution becomes unacceptable. This is especially critical for minimum-feature transistors, where it is desirable to use high V_{dd} to obtain a reasonable

current. This problem occurs even for the "injection error-free" method of [5]. Moreover, the method is "error-free" only for the linear device under test. For nonlinear capacitors it suffers from charge injection too.

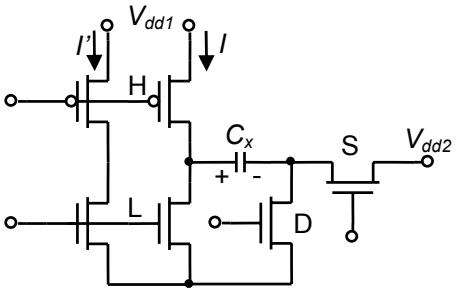


Figure 5. Modified CBCM method.

The proposed modification of the CBCM method is applicable to the measurement of floating devices. Two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the device under test (C_x). One source is swept while the other is kept constant, and vice versa. For each point of the characteristic a minimum voltage amplitude and thereby a minimum DC current are guaranteed. The principal schematic of the proposed test structure is shown in Fig. 5. The method inherits the charge injection problems of the original CBCM.

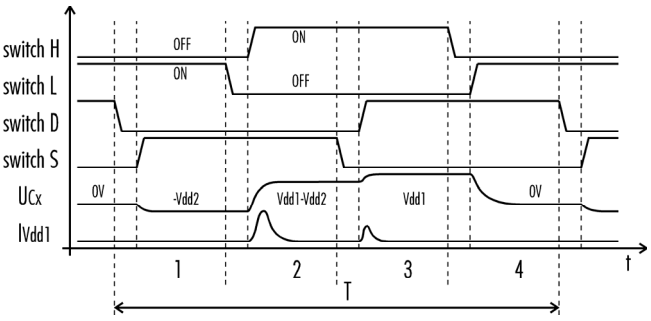


Figure 6. Waveforms of signals in modified CBCM method.

The basic principle of CBCM with the main (right) and compensation (left) switches as shown in Fig. 1 is the same also for the modified method. The DC source V_{dd} was renamed V_{dd1}. The main difference is in the negative terminal of the measured object. The ground connection is replaced by the switch D and the node can be additionally connected to another DC source V_{dd2} by the bidirectional switch S.

One period of controlling signals can be divided into four non-overlapping phases, Fig. 6. During phase 1 the measured capacitor is charged to a negative voltage (seen on its terminals) from the source V_{dd2} through the switches L and S. During phase 2, L is switched off and S remains switched on. Activating the switch H causes charging the capacitor to the voltage V_{dd1}-V_{dd2}. The charge drawn is counted by the ammeter. The voltage changes for V_{dd1}. During phase 3, S is switched off and the capacitor is charged to V_{dd1} through the switch D. The voltage changes for V_{dd2} and the charge drawn is again counted by the ammeter. During the last phase C_x is discharged.

The capacitor voltage varies during one period from $-V_{dd2}$ to V_{dd1} and the charge variation can be determined from the measured current as

$$\Delta Q(V_{dd2}, V_{dd1}) = \frac{I - I'}{f} = \int_{-Vdd2}^{Vdd1} C_x dv \ . \qquad (8)$$

Let us start the reconstruction of Q-v characteristic for negative voltages across C_x, Fig. 7a. The source V_{dd1} is held constant while the source V_{dd2} is swept. The capacitor charge is then

$$Q(-V_{dd2}) = -\int_{-Vdd2}^{0} C_x dv = -\int_{-Vdd2}^{Vdd1} C_x dv + \int_{0}^{Vdd1} C_x dv \ . \qquad (9)$$

Combining (8) and (9) we obtain finally

$$Q(-V_{dd2})_{Vdd1=const} = \Delta Q(0, V_{dd1}) - \Delta Q(V_{dd2}, V_{dd1}) \quad (10)$$

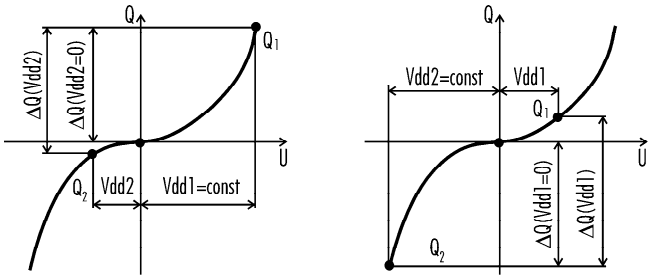
and similarly for the positive voltage

$$Q(V_{dd1})_{Vdd2=const} = \Delta Q(V_{dd2}, V_{dd1}) - \Delta Q(V_{dd2}, 0) \ . \quad (11)$$

Thus the device can be characterized in both polarities, Fig. 7. The dynamic capacitance $C_x(v)$ is then

$$C_x = dQ(v)/dv \ . \qquad (12)$$

Since (12) amplifies random errors, the technique of averaging has been used to smooth $Q(v)$.



a) b)

Figure 7. Reconstruction of Q-v characteristic.

IV. Test Chip Design

The modified CBCM method was implemented in a test-chip to verify its functionality and to characterize nonlinear MOS-gate capacitors and compensation structures. The chip was manufactured in the 3.3V AMIS I3T80 0.35 μm process.

The test-chip consists of 64 test-cells, whose principal schematic is shown in Fig. 5. Each cell is connected to the device under test (MOS capacitor, metal-metal capacitor or

external device). The block diagram of the whole chip is shown in Fig. 8.

Since the power supply voltages vary from 0 to 3.3 V, the correct driving voltages for MOSFET switches *H*, *L*, *D* and *S* are obtained using the level-shifters supplied from constant-voltage sources relative to *Vdd1* and *Vdd2*.

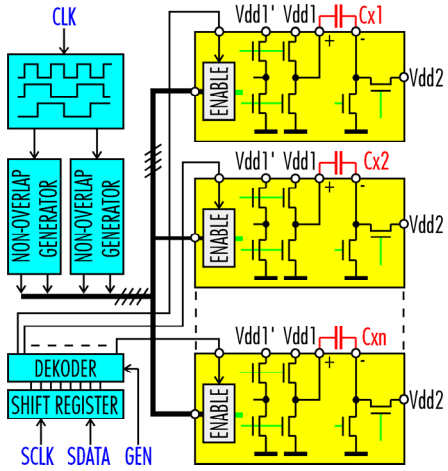


Figure 8. Block diagram of test-chip.

The test-cell topology is universal. It is just the switching sequence generated in the digital unit that determines the actual measuring method. Besides the modified CBCM it is possible to generate sequences for method of [5].

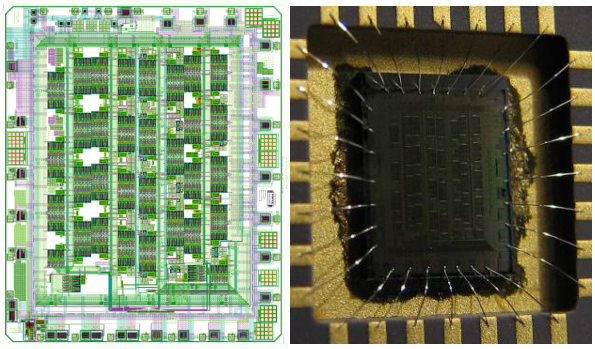


Figure 9. Top layout and die photograph of test-chip.

The main purpose of developing the method was to characterize nonlinear MOS gate capacitors. Such capacitors provide a higher specific capacitance per unit area and do not require additional masks, but the nonlinearity must be carefully compensated. Fig. 10 shows the Q-v and C-v characteristics measured for a 1µm x 1µm NMOS transistor. The clock generator frequency was set to 10 MHz.

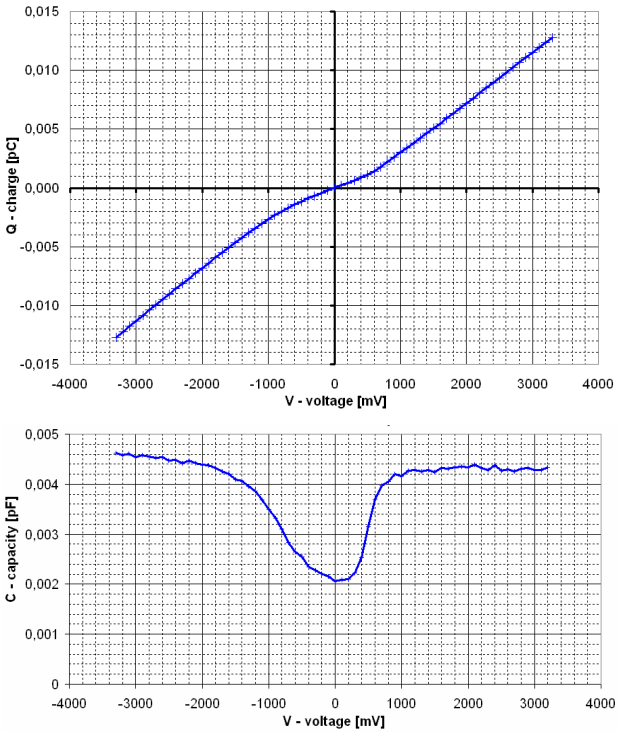


Figure 10. Measured Q-v and C-v characteristics of MOS gate.

V. Conclusion

A modification of the CBCM method for nonlinear capacitance characterization was proposed. Just two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the object being measured. A test-chip implementing the method was designed and manufactured in the 0.35µm CMOS process.

References

[1] J.C. Chen, B.W. McGaughy, D. Sylvester, and C. Hu, "An on-chip attofarad interconnect charge-based capacitance measurement (CBCM) technique", In: Proc. of IEDM'96, 1996, pp. 69-72.

[2] J. Chen, D. Sylvester, Ch. Hu, "An On-Chip, Interconnect Capacitance Characterization Method with Sub-Femto-Farad Resolution", IEEE Trans. on Sem. Manufacturing, Vol. 11, No. 2, 1998, pp. 204-210.

[3] L. Vendrame, L. Bortesi, A. Bogliolo, "Accuracy Assessment and Improvement of On-Chip Charge-Based Capacitance Measurements", In: Proc. of the 7th IEEE SPI Workshop, 2002.

[4] Y. W. Chang, H. W. Chang, C.H. Hsieh, H.C. Lai, T.C. Lu, W. Ting, J. Ku, C.Y. Lu, "A novel simple CBCM method free from charge injection-induced errors", IEEE Electron Device Letters, Volume 25, No 5, 2004, pp. 262-264.

[5] Y.W. Chang, H.W. Chang, T.C. Lu, Y.C. King, W. Ting, Y.H.J. Ku, C. Y. Lu, "Charge-Based Capacitance Measurement for Bias-Dependent Capacitance", IEEE Electron Device Letters, Volume 27, No 5, 2006, pp. 390-392.

[6] B.J. Sheu, C.M. Hu, "Modeling the Switch-Induced Error Voltage on a Switched Capacitor", IEEE Transaction on Circuit and Systems, vol. 30, No 12, 1983, pp. 911-913.

[7] Y. Ding, R. Harjani, "A Universal Analytic Charge Injection Model", In: Proc. of ISCAS 2000, Geneva, 2000, pp. I-144 – I-147