

Optimization of CDTA-based circuits simulating ladder structures

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Abstract: Rules of mutual transformation of equivalent CDTA-based circuit structures are described. After the transformation into the so-called structure with grounded impedances, several optimization methods can be applied, and then it is possible to pass to a simpler circuit, applying backward transformation. The procedures are demonstrated on an example of current-mode LeapFrog structure.

Keywords: - Current mode, CDTA, optimization

1 INTRODUCTION

The CDTA (Current-Differencing Transconductance Amplifier) building block has been introduced in [1]. It has difference low-impedance current inputs p and n . The difference of input currents, multiplied by a current gain b , flows out of the z – terminal into an outside load. The current gain b is commonly equal to 1. However, it can be controlled electronically. The voltage across the z – terminal is transformed into current I_x through an internal transconductance and it is conducted to the x – terminals. The concluding part of the element is a multi-output Operational Transconductance Amplifier.

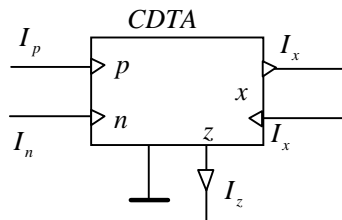


Fig. 1: Schematic symbol of CDTA, DIDO type.

Regarding the input terminals p and n and the output terminals x , and using the terminology introduced in [2], the CDTA behaves as a difference-input multiple-output (DIMO) current amplifier. Concretely, the schematic symbol in Fig. 1 corresponds to the DIDO type (Differential Input Differential Output). For concurrent directions of currents I_x , the circuit should be called DICO (Differential Input Common Output).

In [3,4], some ideas of CDTA applications are described, with a view to active filters. In the paper, the basic rules for a potential optimization of DCTA-based circuits will be stated. The rules and procedures will be demonstrated on active structures which simulate passive ladder filters.

2 EQUIVALENT CIRCUITS CONTAINING CDTAs

Circuits designed with CDTA elements usually have to be optimized according to various criteria, e.g. maximum dynamic range, minimum spread of capacitances or transconductances, optimum impedance levels, etc. Certain circuit structures exist where the given optimizations can be performed with various degrees of freedom. That is why it is desirable to know the rules of transformation between equivalent circuit structures. The so-called structures with grounded immittances are appropriate for optimization. In general, these structures consist of CDTA elements, current amplifiers and immittances with one outlet either grounded or connected to ground potential (i.e. to some current input of CDTA or virtual ground of OpAmp).

The equivalence of circuits in Fig. 2 (a) can be checked by a simple computation: If a current amplifier with gain K_I exists in the negative feedback loop of CDTA element, the loop can be removed and replaced by a grounded admittance bg_mK_I , connected to the z -terminal.

Both structures in Fig. 2 (a) belong to grounded-immittance structures. The equality of input currents I results in the equality of currents I_x and voltages V_z . Note that both structures differ in currents I_n and I_z .

Another equivalence is given in Fig. 2 (b). By means of this equivalence, floating immittances can be transformed into grounded immittances.

In Fig. 2 (b), only the second circuit belongs to the class of grounded-immittance structures. The equality of currents I_{n1} , I_{p1} , I_{n2} , and I_{p2} in both structures results in the equality of voltages V_z and currents I_x , not the equality of currents I_z .

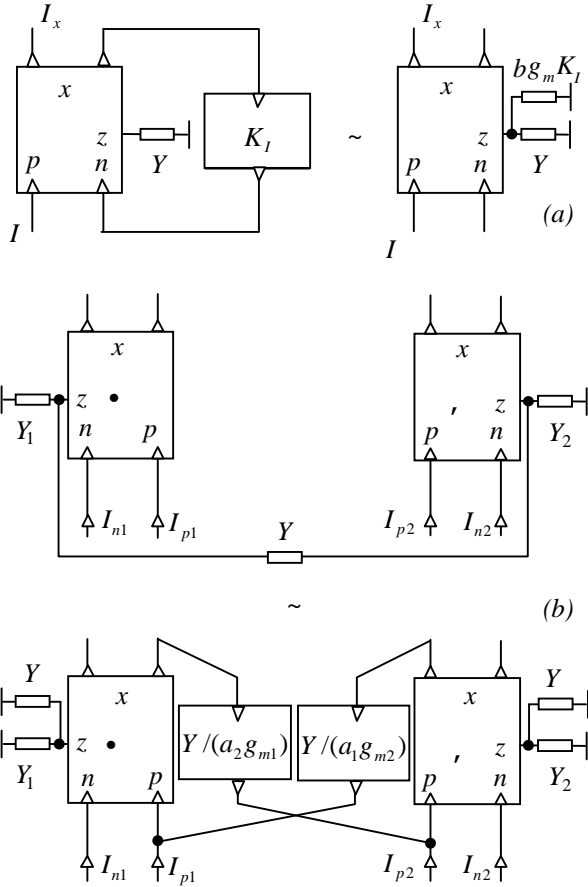


Fig. 2: Removal of the feedback path (a), floating immittance (b).

3 OPTIMIZATION RULES

For circuits with grounded immittances, several regularities hold which can be formalized in the Propositions below. It should be noted that some of the regularities are also valid for certain circuits with floating immittances. Additional regularities which are applied only for some concrete circuit structures are not discussed. They can be derived from the flow graphs of these structures. The Propositions below can generally be used to optimize grounded structures.

Proposition 1:

We increase k -times the transconductance g_m of CDTA and decrease k -times all the impedances, connected to the z -terminal of this CDTA. Then the voltages and currents in the whole circuit remain unchanged, excepting voltage V_z , which decreases k -times.

This Proposition can be used to modify voltage at the z -terminal of a given CDTA without affecting the rest of voltages and currents in the circuit.

Proposition 2:

We increase k -times the transconductance g_m of CDTA and decrease k -times all the current transfers from the x -

terminals of this CDTA into the other circuit nodes. Then the voltages and currents in the whole circuit remain unchanged, excepting current I_x , which increases k -times.

Note 1: When the p or n input of another CDTA is connected to the x -terminal of CDTA, then the above current gain from the x -terminal will be decreased by lowering the current gain b of a connected CDTA.

Note 2: When the p or n input of another CDTA is connected to the x -terminal of CDTA and the connected CDTA is simultaneously fed by input current, it is necessary to amplify this current k -times.

Note 3: When a passive current divider is fed from the x -terminal, voltage V_x can also be changed. For a CDTA-based current divider, the voltage V_x is zero.

This Proposition can be used to modify the level of currents I_x of a given CDTA without affecting the rest of voltages and currents in the circuit.

Proposition 3:

We increase k -times the current gain b of CDTA and decrease k -times the transconductance g_m of this element. Then the voltages and currents in the whole circuit remain unchanged, excepting current I_z and voltage V_z , which increase k -times.

This Proposition can be used to modify the level of voltage V_z of a given CDTA without affecting the rest of voltages and currents in the circuit.

Proposition 4:

We increase k -times the current gain b of CDTA and decrease k -times all the impedances connected to the z -terminal of this element. Then the voltages and currents in the whole circuit remain unchanged, excepting current I_z , which increases k -times.

This Proposition can be used to modify the impedance level at the z -terminal of a given CDTA without affecting the rest of voltages and currents in the circuit.

During circuit optimization using the above rules, it is convenient to follow three steps:

1. We transform the circuit into a structure with grounded impedances.
2. We apply some of the rules from Propositions 1 to 4.
3. We transform the structure with grounded impedances back into a structure with floating impedances.

The purpose of step 1 is to move into a structure where Propositions 1 to 4 are true. However, this structure is generally more complicated than the original one (see Fig. 2(b)). The purpose of step 3 is thus to return to a simpler structure. Nevertheless, due to modifications during the optimization in step 2, we usually do not reach a full simplification to the original structure.

4 DEMONSTRATION

4.1 Preliminary design of CDTA-based ladder filter

Consider the ladder filter in Fig. 3. This 6th-order current-mode Chebyshev bandpass filter with a central frequency of 10MHz, 1.4MHz bandwidth and 0.1dB passband ripple was designed using the NAFID program. The R , L , and C values are as follows:

$$R_1=R_2=100\Omega, C_1=C_5=1.48\text{nF}, C_2=C_4=159\text{pF}, \\ C_3=1.5\text{nF}, L_1=L_3=0.155\mu\text{H}, L_2=0.139\mu\text{H}.$$

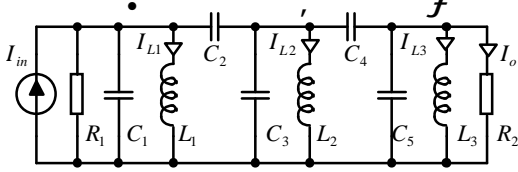


Fig. 3: 6th-order bandpass ladder filter with coupled circuits.

For selected currents and node voltages, well-known equations can be compiled as a basis of flow-graph simulation by means of integrating structures:

$$V_1 = \frac{1}{G_1 + sC_1} [I_{in} - I_{L1} - I_{C2}], \quad V_2 = \frac{1}{sC_3} [I_{C2} - I_{C4} - I_{L2}], \\ V_3 = \frac{1}{G_2 + sC_5} [I_{C4} - I_{L3}], \quad I_{L1} = \frac{V_1}{sL_1}, \quad I_{L2} = \frac{V_2}{sL_2}, \quad I_{L3} = \frac{V_3}{sL_3} \quad (1)$$

These equations are conformable with the active structure in Fig. 4. In the first step, let us consider the internal current gains b of all CDTA elements to be 1. Equations for I_{L1} , I_{L2} and I_{L3} follow from Fig. 4:

$$I_{Lk} = g'_{mk} V_{Ck} = g'_{mk} \frac{g_{mk} V_k}{sC_{Lk}} = \frac{V_k}{s \frac{C_{Lk}}{g_{mk} g'_{mk}}}, \quad k = 1, 2, 3. \quad (2)$$

From a comparison of equations (2) and (1) it results that the inductors in Fig. 4 are simulated by CDTA elements and by capacitors C_{Lk} according to the equations

$$L_k = \frac{C_{Lk}}{g_{mk} g'_{mk}}, \quad k = 1, 2, 3, \quad (3)$$

where g_{mk} and g'_{mk} are transconductances of CDTAs.

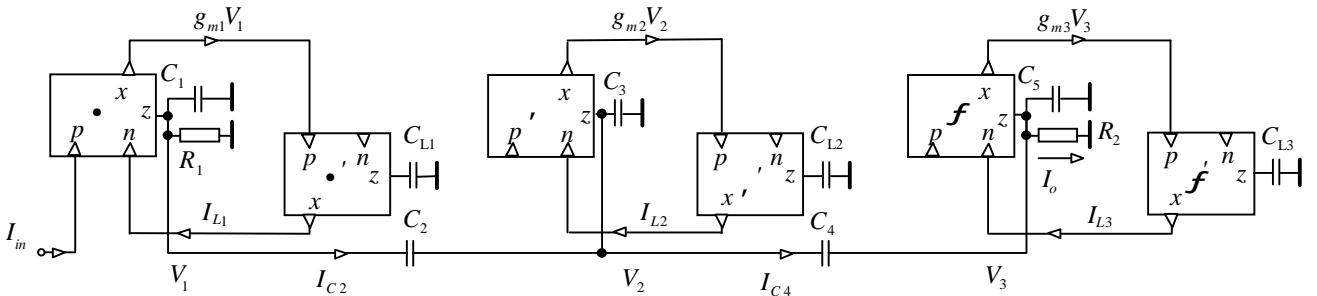


Fig. 4: CDTA-based circuit structure simulating RCL ladder filter in Fig. 3.

In the first design step, we choose all the transconductances of all CDTAs to be identical:

$$g_m = \frac{1}{R_1} = \frac{1}{R_2} = 10\text{mS}.$$

Then capacitances C_{Lk} will be according to (3)

$$C_{L1} = C_{L3} = 15.5\text{pF}, \quad C_{L2} = 13.9\text{pF}.$$

The filter has preliminarily been designed. A computer simulation of its behaviour follows.

4.2 Computer simulation of circuits with CDTAs

The following models were created for computer simulation and optimization of circuits containing CDTAs:

- Behavioral models of ideal CDTA elements, current amplifiers and splitters for symbolic, semisymbolic and numerical analyses in the SNAP program [5].
- The SPICE model of CDTA. This model consists of two parts: The model of a current source I_z controlled by the difference of currents I_p and I_n is adopted from the model of CDBA element [6]. For linear small-signal analysis, all three currents cannot exceed 30mA. The transconductance amplifier is modeled by the SPICE model of the commercial 275MHz amplifier MAX435.

The optimization of a preliminarily designed filter will be shown in two basic stages:

- Dynamic-range and impedance-level optimization by means of the SNAP program.
- Final simulation and design verification by SPICE.

4.3 Optimization procedures

The results of SPICE simulation of the filter from Fig. 4 are shown in Fig. 5. A comparison with the frequency response of the original ladder RCL filter yields a significant frequency shift in the response of CDTA-based filter. However, it is not useful to compensate it during this first stage of optimization. This phenomenon is caused by the relatively small values of C_{L1} , C_{L2} , and C_{L3} , which get near the parasitic capacitances of the SPICE model of CDTA.

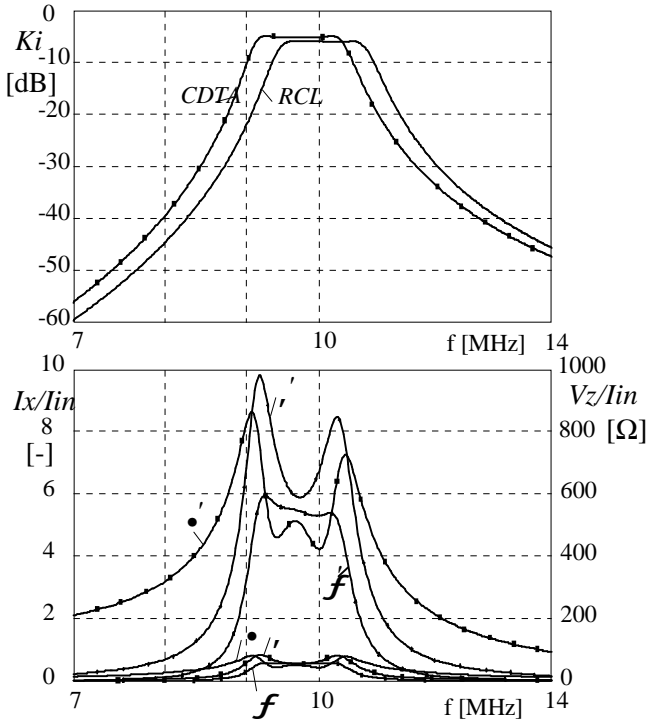


Fig. 5: Frequency response of the RCL ladder filter in Fig. 3 (RCL) and the simulated response of CDTA-based LeapFrog structure according to Fig. 4 (CDTA). Below are transfers from the input current to current outputs (x outlets) or voltage outputs (z outlets) of individual CDAs.

As shown in Fig. 5, the filter exhibits a large spread of maximum current transfers into the x -terminals of individual CDAs. Because of the equal transconductances in this design stage (10mS), these curves also represent transfers from input I_{in} into outputs V_z . That is why we should focus the optimization on the following:

- Decreasing the impedance levels at the z -terminals of CDAs No. 1', 2', and 3'. Then the voltages across these terminals will be lowered to the levels at the z -terminals of the remaining CDAs. Simultaneously it will result in an increase in capacitances C_{L1} , C_{L2} , and C_{L3} with subsequent reduction of undesired shift of the frequency response. In other words, it is necessary to optimize the upper bound of dynamic range of voltages V_z .
- Equalizing the current transfers from input into the x -outputs of individual CDAs. In other words, it is necessary to optimize the upper bound of dynamic range of currents I_x .

A SNAP analysis of the filter in Fig. 4 leads to similar results as in the SPICE simulation with the difference that the frequency responses of the CDTA and RCL filters are practically identical due to idealized models of CDAs. The values of transfer maxima in Fig. 5, scanned by SNAP program, are summarized in Table 1.

CDTA No.	I_x/I_{in} [-]	V_z/I_{in} [Ω]
1	0.7439	74.39
2	0.7300	73.00
3	0.5000	50.00
1'	8.143	814.3
2'	8.605	860.5
3'	5.343	534.3

Table 1: Maxima of shapes in Fig. 5 obtained by SNAP program.

It results from Table 1 that for input current up to 10mA, voltages at the z -terminals of individual CDAs would be from 0.5V (CDTA No. 3) to 8.6V (CDTA No. 2'), and output currents from the x -terminals would be from 5mA to 86mA. However, the last mentioned value exceeds the permitted value of the terminal current of CDTA in terms of the SPICE model (30mA). That is why an optimization of the upper bound of dynamic range is necessary both for currents I_x and voltages V_z (for the sake of low voltages and small spread of their levels).

To obtain more degrees of freedom for the optimization, let us transform the original filter structure in Fig. 4 into a structure with grounded impedances in Fig. 6. The embedded current amplifiers with gains $sC/(bg_m)$ can be implemented, for instance, by a circuit with CDTA element according to [2].

Optimization of the upper bound of current-voltage transfers into z -terminals to value $V_z/I_{in} = 100\Omega$
(for an input current of up to 10mA, voltages across the z -terminals will not exceed 1V).

Proposition 1 will be used for optimization as follows:

$$C_{12} \rightarrow 0.7439C_{12}, R_1 \rightarrow R_1/0.7439, g_{m1} \rightarrow 0.7439g_{m1}$$

Accordingly, C_{234} and g_{m2} will be changed 0.73times, C_{45} and g_{m3} will be halved, R_2 will be doubled, etc. The resulting values after this optimization step can be found in column „2“ of Table 2.

Optimization of the upper bound of current-current transfers into x -terminals to value $I_x/I_{in} = 1$
(for an input current of up to 10mA, currents of the x -terminals will not exceed 10mA).

Proposition 2 including **Notes 1** and **2** will be used for optimization as follows:

$$g_{m1} \rightarrow g_{m1}/0.7439, b'_1 \rightarrow 0.7439b'_1,$$

$K_{I1} \rightarrow 0.7439K_{I1} \dots$ will be done e.g. by changing capacitance C_2 inside block K_{I1} ,

$$g'_{m1} \rightarrow g'_{m1}/8.143, R_1 \rightarrow 8.143R_1, C_{12} \rightarrow C_{12}/8.143,$$

$$K_{I2} \rightarrow K_{I2}/8.143,$$

$I_{in} \rightarrow I_{in}/8.152 \dots$ will be done by including a current attenuator in the filter input.

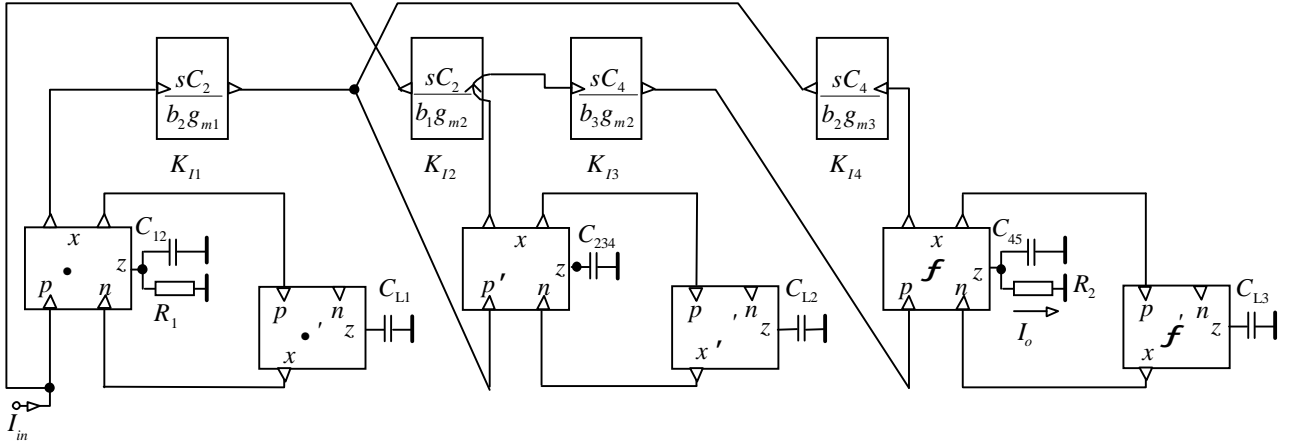


Fig. 6: Circuit from Fig. 4 after transformation according to Fig. 2(b) into a structure with grounded impedances. At this stage, current gains b of all the CDTAs are equal to 1.

The current levels for the remaining CDTAs will be modified accordingly. The resulting values of circuit elements after this optimization step are summarized in column „3“ of Table 2.

The SNAP simulation (see Fig. 7) confirms that both the voltage and current dynamic ranges are optimized.

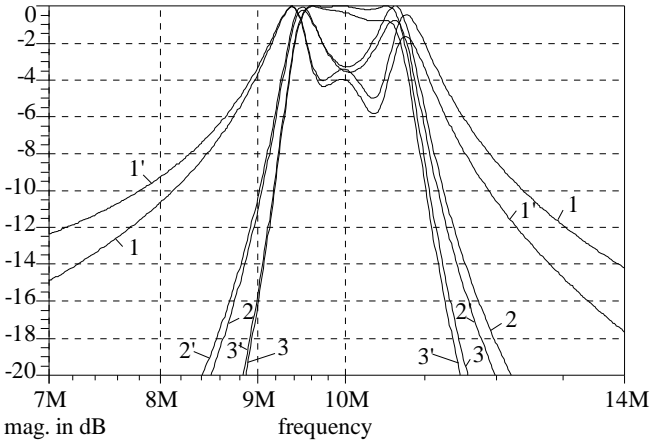


Fig. 7: Frequency responses of current transfers I_{xi}/I_{in} after dynamic range optimization. Frequency responses V_z/I_{in} are similar to maxima settled to a level of 100Ω .

Now we can simplify the structure in Fig. 6 by transforming it into a structure with floating impedances according to Fig. 2(b).

The current amplifiers with transfer functions K_{I1} and K_{I2} contain capacitors with capacitances of 13.7pF and 14.3pF . According to Fig. 2(b), block K_{I1} can be removed, block K_{I2} will change its capacitance to $(14.3-13.7)\text{pF}=0.6\text{pF}$, a capacitance of 13.7pF will be subtracted from capacitances C_{12} and C_{234} , and a floating capacitance of 13.7pF will be connected between the z -terminals of CDTAs No. 1 and 2. Computer simulation then proves that block K_{I2} with a negligible working capacitance of 0.6pF can be removed without affecting the resulting frequency response.

In a similar way, block K_{I4} can be removed, block K_{I3} will modify its capacitance to $(21.7-9.2)\text{pF} = 12.5\text{pF}$, a capacitance of 9.2pF will be subtracted from C_{234} and C_{45} and regarded as a floating capacitance between the z -terminals of CDTAs No. 2 and 3. The final circuit is shown in Fig. 8 and the corresponding element values are summarized in column “4” of Table 2.

Some of the working capacitances are too small. It is advisable to decrease the impedance level approximately 5 times. The new values are given in column „5“ of Table 2. Note that decreasing the impedance level 5 times caused lowering the voltage levels 5 times compared with the original design. That is why voltages of up to 200mV across the z -terminals will now correspond to an input current of 10mA .

Fig. 8 shows a possible filter simplification via replacing active block K_{I3} by a passive current divider.

SPICE simulation of the optimized filter

The results of simulation of the optimized filter from Fig. 8 are given in Fig. 9. Frequency responses exhibit a good agreement with both the response of the original RCL ladder filter and the optimization intentions.

5 Conclusion

The CDTA circuit element enables easy current-mode „Leap-Frog“ simulation of RCL ladder filters. The above circuit equivalences and rules enable us to optimize the designed circuit according to various criteria using more degrees of freedom.

Acknowledgments

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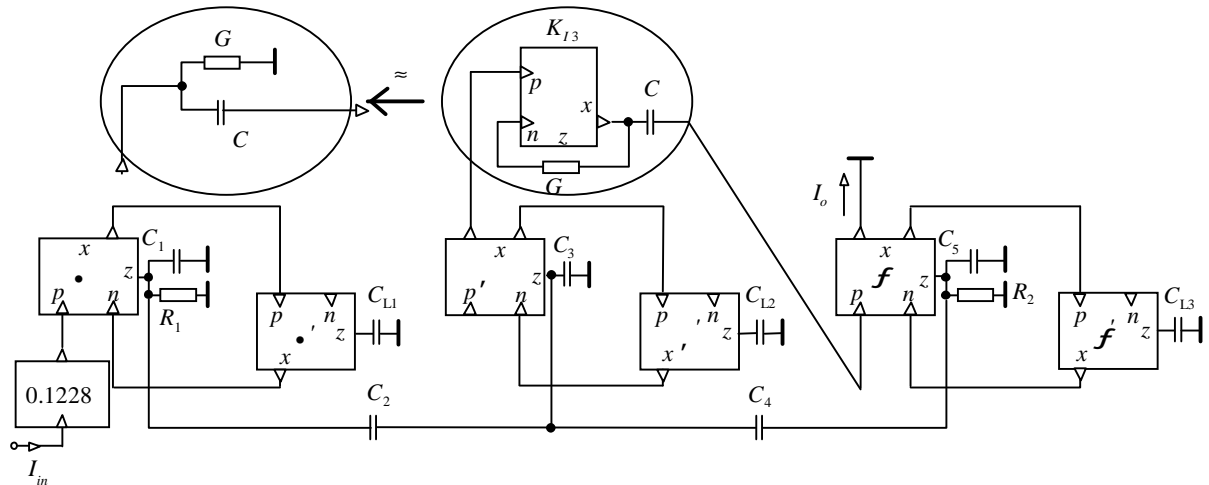


Fig. 8: Filter structure after optimization.

	1	2	3	4	5
g_{m1}	10m	7.439m	10m	10m	50m
b_1	1	1	1	1	1
g_{m2}	10m	7.3m	10m	10m	50m
b_2	1	1	1	1	1
g_{m3}	10m	5m	10m	10m	50m
b_3	1	1	1	1	1
g'_{m1}	10m	81.43m	10m	10m	50m
b'_1	1	1	0.7439	0.7439	0.7439
g'_{m2}	10m	86.05m	10m	10m	50m
b'_2	1	1	0.73	0.73	0.73
g'_{m3}	10m	53.43m	10m	10m	50m
b'_3	1	1	0.5	0.5	0.5
C_1	1480	-	-	136	680
C_2	159	-	-	13.7	68.5
C_3	1500	-	-	131.3	656.5
C_4	159	-	-	9.2	46
C_5	1480	-	-	144.2	721
C_{L1}	15.5	126.2	126.2	126.2	637
C_{L2}	13.9	119.6	119.6	119.6	598
C_{L3}	15.5	82.8	82.8	82.8	414
R_1	100	134.4	1094.6	1094.6	218.9
R_2	100	200	1068.6	1068.6	213.7
C_{12}	1639	1219.3	149.7	-	-
C_{234}	1818	1327.1	154.2	-	-
C_{45}	1639	819.5	153.4	-	-
K_{11} :	C_2	159	159	13.7	-
	g_{m1}	10m	10m	10m	-
K_{12} :	C_2	159	159	14.3	0.6 \rightarrow 0
	g_{m2}	10m	10m	10m	-
K_{13} :	C_4	159	159	21.7	12.5
	g_{m2}	10m	10m	10m	10m
K_{14} :	C_4	159	159	9.2	-
	g_{m3}	10m	10m	10m	-

Tab. 2: Development of the C [pF], R [Ω], g_m [mS] parameters of the filter in Fig. 4, 6, 8 during optimization. The numbers in columns are: **1** before optimization, **2** after optimizing the voltages at z -terminals, **3** after optimizing the current transfers into x -terminals, **4** after transforming the grounded impedances into floating ones in Fig. 8, **5** after modifying the impedance levels.

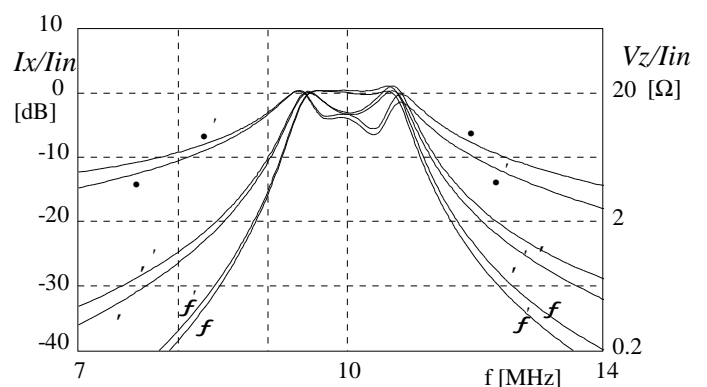


Fig. 9: SPICE simulation of frequency responses of the optimized filter in Fig. 8 (the variant with a passive current divider). The values of circuit elements are in column "5" of Table 2.

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