Simulating Arbitrary Transfer Function by CDTA-Based Current Divider

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Abstract: A novel structure of an active filter containing CDTA building blocks is described. This current-mode structure can model an arbitrary transfer function on the principle of simulation of high-order immittances. A simple design procedure following directly from the coefficients of transfer function is described.

Keywords: - Current mode, CDTA, immittance

1 Introduction

Non-cascade filters are known which model an arbitrary transfer function on the principle of current divider and simulation of high-order immittances [1]. This smart "modular" filter structure is accompanied by its well-known drawbacks, namely higher sensitivities and complicated design procedures.

The problem of sensitivity properties concerns particularly the high sensitivities of zeros and poles to the coefficient values of transfer function. In general, these sensitivities increase with the order of transfer function and with the quality factors of zeros and poles. That is why this type of synthesis is inadvisable for filters with relatively high orders and for such approximations of frequency responses that lead to comparatively high quality factors of 2nd-order subsections.

In other cases, whose typical representative can be, for example, a 5th-order filter according to Bessel, Butterworth or the inverse Chebyshev approximation, with quality factors of up to 10, the synthesis from the transfer function can bring interesting results. Then it is suitable to look for such circuit solutions that enable eliminating the other, often-mentioned drawback, i.e. complicated design procedure.

The circuit structure given below uses a CDTA (Current Difference Transconductance Amplifier) active element [2-5]. The filter consists of a general admittance Y_0 and of the cascading blocks, each of which includes a CDTA element and an additional impedance. The given block then simulates an admittance that is directly proportional to the admittance of the preceding block, to the additional impedance in the given block, and to the transconductance of the given CDTA element. This structure leads to simple design procedures, which will be demonstrated on the example of a concrete 5th-order 50MHz lowpass filter.

2 CDTA element

The principle of CDTA element is described in [2], [3]. The summary is given in Fig. 1. This element consists of a difference-input current amplifier and a cascading multi-output OTA (Operational Transconductance Amplifier). In Fig. 1, the difference outputs are always given. The OTA input is led out to an auxiliary *z*-terminal.

Gain b of the current amplifier and transconductance g_m of the OTA are either fixed or electronically adjustable to control filter parameters.

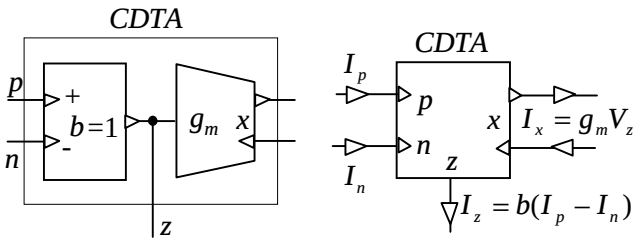

Fig. 1: Principial model of CDTA element, its schematic symbol with designated terminal currents.

3 Generalized current dividers with CDTA elements

Let us consider the circuit in Fig. 2 (a) containing n CDTA elements.

The admittance Y_0 is connected to the ground potential by one outlet through the *p*-terminal of CDTA No 1. That is why at the input gate to which the input source is connected it behaves like simulated admittance $Y_{s0} = Y_0$ (see Fig. 2b).

Current I_1 is given by the product of transconductance g_{m1} of CDTA No 1 and the voltage at impedance Z_1, which is equal to current I_0 multiplied by current gain b_1 of CDTA No 1 and by impedance Z_1. The following is true:

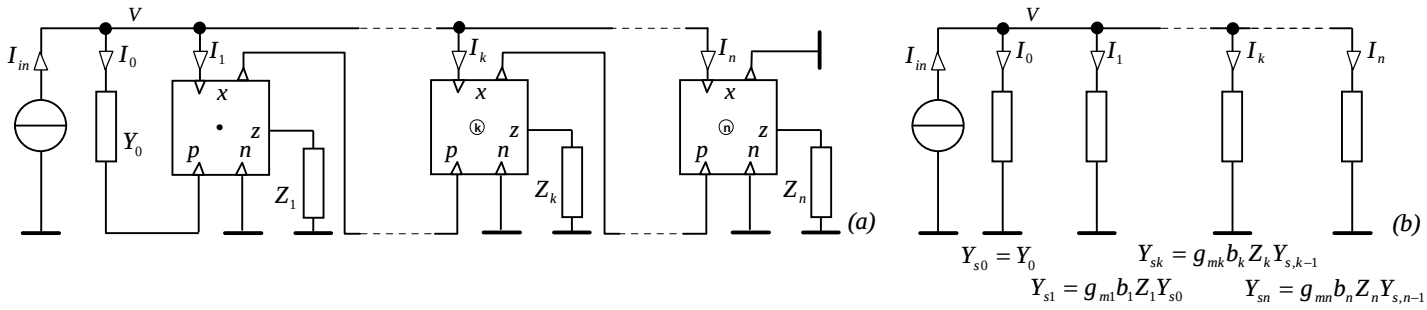

Fig. 2: (a) generalized current divider with CDTA elements, (b) its equivalent model.

$$I_1 = g_{m1} b_1 Z_1 I_0 = g_{m1} b_1 Z_1 Y_0 V .$$

CDTA No 1 loads the input gate in the same way as simulated admittance $Y_{s1} = g_{m1} b_1 Z_1 Y_0$.

Similarly, CDTA No k loads the input gate and simulates the admittance

$$Y_{sk} = g_{mk} b_k Z_k Y_{s,k-1},\ Y_{s0} = Y_0,\ k = 1, 2, \ldots n. \quad (1)$$

Recurrent formula (1) has the following solution:

$$Y_{sk} = Y_0 \prod_{i=1}^{k} g_{mi} b_i Z_i ,\ k = 0, 1, \ldots n. \quad (2)$$

All the simulated admittances of the current divider in Fig. 2 (b) are proportional to admittance Y_0. That is why the dividing ratios will not depend on this admittance:

$$\frac{I_k}{I_{in}} = \frac{Y_{sk}}{\sum_{l=0}^{n} Y_{sl}} = \frac{\prod_{i=1}^{k} g_{mi} b_i Z_i}{\sum_{l=0}^{n} \prod_{i=1}^{l} g_{mi} b_i Z_i},\ k = 0, 1, \ldots n. \quad (3)$$

Consider that all impedances Z_k, $k = 1, 2, \ldots n$, will be implemented by capacitors, i.e.

$$Z_k = \frac{1}{sC_k},\ k = 1, 2, \ldots n. \quad (4)$$

Substituting (4) into (3) and re-arranging yield the current transfers as follows:

$$\frac{I_k}{I_{in}} = \frac{c_{n-k} s^{n-k}}{\sum_{i=0}^{n} d_i s^i},\ k = 0, 1, \ldots n, \quad (5)$$

where

$$c_k = d_k = \prod_{i=1}^{n-k} \frac{g_{mi} b_i}{C_i},\ k = 0, 1, \ldots n. \quad (6)$$

Via weighted summation of transfer functions (5), an arbitrary n^{th}-order transfer function can be implemented. This summation can be accomplished by linear combination of currents flowing out of the z-terminals of individual CDTA elements.

4 Filter design from coefficients of transfer function

Let us consider the n^{th}-order transfer function

$$K(s) = \frac{\sum_{i=0}^{n} A_i s^i}{\sum_{i=0}^{n} B_i s^i},\ B_n = 1 \quad (7)$$

which is given as input data for filter synthesis.

Comparing equations (5), (6), and (7) and considering other design requirements, the following procedure takes place:

(a) Design of parameters of CDTA elements

Current gains b_k and transconductances g_{mk} will be set equal for all CDTA elements. The recommended values are as follows:

$$b = 1,\ g_m \approx B_{n-1} C, \quad (8)$$

where C is the estimated dimension of working capacitances in the filter.

(b) Design of working capacitances

Capacitances C_1 to C_n, which represent impedances Z_1 to Z_n in Fig. 2 (a), will be designed according to the following equations:

$$\begin{aligned} C_1 &= g_{m1} b_1 \frac{B_n}{B_{n-1}} = g_m \frac{1}{B_{n-1}} \\ C_2 &= g_{m2} b_2 \frac{B_{n-1}}{B_{n-2}} = g_m \frac{B_{n-1}}{B_{n-2}} \\ &\ldots \\ C_k &= g_{mk} b_k \frac{B_{n-k+1}}{B_{n-k}} = g_m \frac{B_{n-k+1}}{B_{n-k}} \\ &\ldots \\ C_n &= g_{mn} b_n \frac{B_1}{B_0} = g_m \frac{B_1}{B_0} \end{aligned} \quad (9)$$

(c) Implementation of the numerator of transfer function (7)

Current I_k, $k = 0, 1, .., n$, flowing from the z-terminal of CDTA No k into the ground, will be led into the low-impedance input of the current amplifier with a gain of

$$K_{ik} = \frac{A_{n-k}}{c_k},\ k = 0, 1, .., n. \qquad (10)$$

The amplifier will be certainly omitted when the corresponding gain is zero or it will be replaced by short connection in the case of unity gain.

The outputs of the appropriate current amplifiers are then led to a summing node from which the output current flows into the ground (see Fig. 3).

(d) Design of admittance Y_0

Even if the current transfers are independent of admittance Y_0, both the value and the character of this impedance affect the input and voltage levels and other real properties of active filter. Furthermore, a DC offset current flowing through this admittance can cause serious stability problems, because this current is copied directly into capacitor C_1. Considering these and other reasons, it is suitable to implement admittance Y_0 by a capacitor. The capacitance value should be chosen with respect to the required impedance levels and the corresponding voltage level at the input gate, as well as to the terminal currents of CDTAs.

(e) Filter optimization

In the case of non-optimal values of parameters g_{mk}, C_k, k = 1, 2, .., n from the tentative design, it is possible to modify them in order to preserve the ratios

$$\frac{g_{mk} b_k}{C_k},\ k = 1, 2, ..., n.$$

These variations can but need not change the voltage levels at the *z*-terminals of CDTAs, which can also be optimized in this way. For example, increasing capacitance C_k from a problematic value of 5pF to 20pF must be accompanied by increasing b_k four times or by increasing g_{mk} four times or perhaps by doubling both the parameters. In the first case, the impedance level of the *z*-terminal is decreased, but we increased the current into this terminal accordingly. Thus the *z*-terminal voltage remains unchanged as well as the current through the *x*-terminals, which is derived from this voltage through the transconductance. In the second case, the voltage level at the *z*-terminal decreases four times, but the *x*-terminal current remains constant due to the increased transconductance. In the third case, the voltage at the *z*-terminal decreases two times while I_x will be unchanged.

During the optimization, any prospective change of the current flowing out of the *z*-terminal of CDTA No *k* must be compensated by modifying the corresponding current gain $K_{i,k}$ (see Fig. 3). On the other hand, the above optimization can be controlled with the aim of adjusting $K_{i,k}$ to 1 with subsequent replacement of the current amplifier by short connection.

It is useful to optimize the filter together with its computer simulation. More details about circuit optimization containing CDTA elements is given in [4].

5 Design demonstration

The design objective is a lowpass filter according to the inverse Chebyshev approximation, 50MHz cutoff frequency, 2dB passband ripple, and 40dB guaranteed attenuation above 100MHz. The NAFID program [6] generates results of the approximation task, which are summarized in Table 1.

i	A_i	B_i
0	6.67889E42	6.67889E42
1	0	5.17857E34
2	2.97433E25	2.30507E26
3	0	6.47909E17
4	2.64914E7	1.13865E9
5	0	1

Table 1: Coefficients of transfer function (7) of a filter designed by the NAFID program.

The procedure described in Chapter 4 leads to the filter structure in Fig. 3. This 5th-order filter is implemented by 5 CDTA elements, 6 capacitors, and –in general - 2 current amplifiers or shall we say attenuators. The component values in the first design step are summarized in Table 2, column "1".

The filter simulation has been performed by the SNAP [7], [8] and SPICE programs. The corresponding models are described in [9], [2], [10].

Some results of the SNAP simulation are shown in Fig. 4. It can be seen from the picture that for the input current of 1mA, the voltage at the input gate/*z*-terminals will not exceed a value of 4.5mV/222mV. In other words, both the input source and the „*x*"-outputs of CDTAs

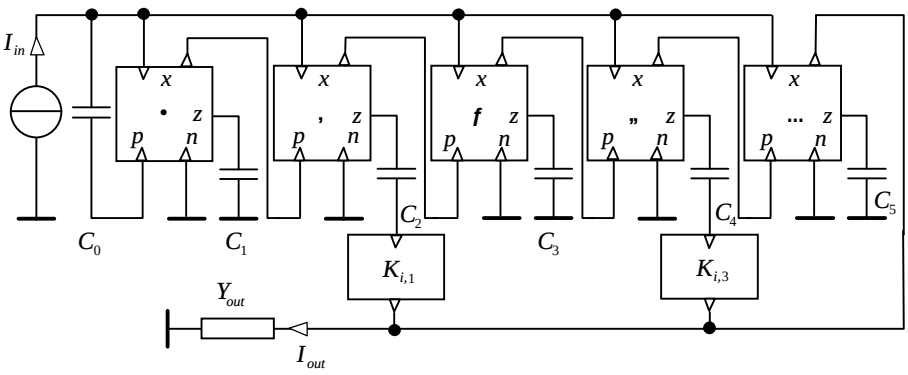

Fig. 3: Designed 50MHz lowpass filter. Component values are in Table 2.

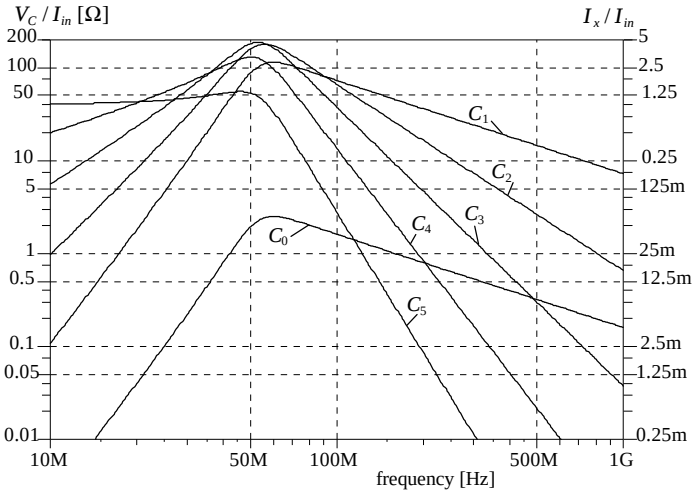

Fig. 4: SNAP simulation: Frequency-dependence of voltages across capacitances and currents at *x*-terminals of preliminary designed filter in Fig. 3. The *x*-current of CDTA No *k* corresponds to the curve of capacitor No *k*.

work into the low-impedance load. It is by virtue of the large value of C_0.

	1	2	3
g_{m1}	25m	114m	31m
b_1	1	1	3.68
g_{m2}	25m	57m	48m
b_2	1	1	1.18
g_{m3}	25m	36m	49m
b_3	1	1	0.741
g_{m4}	25m	23m	33m
b_4	1	1	0.693
g_{m5}	25m	13m	14m
b_5	1	1	0.905
C_0	1n	1n	1n
C_1	22p	100p	100p
C_2	44p	100p	100p
C_3	70p	100p	100p
C_4	111p	100p	100p
C_5	194p	100p	100p
$K_{i,1}$	0.023265	0.02327	0.0197
$K_{i,3}$	0.129027	0.12903	0.1862

Table 2: Development of the C [F], g_m [S] parameters of the filter in Fig. 3 during optimization. The numbers in columns are: **1** before optimization, **2** after optimizing the working capacitances, **3** after optimizing the voltages at the *z*-terminals.

Since the transconductances of all CDTAs have the same value of 25mS, curves $V(C_1)$ to $V(C_5)$ represent also frequency-dependent output currents „I_x“ of the individual CDTAs with the condition that the corresponding voltages are multiplied by 25mS. For an input current of 1mA, the output current maxima are from 1.5mA (CDTA No 5) to 5.6mA (CDTA No 2). In principle, the upper bound of the current dynamic range cannot be optimized in this filter structure. However, we can optimize the upper bound of the *z*-terminal voltages by varying the g_m and *b* parameters according to Chapter 4(e).

In the first optimization step, all the working capacitances C_1 to C_5 are set to an equal value of 100pF (see column “2” in Table 2). To modify the capacitances without affecting the *x*-terminal currents, transconductances g_m must be changed accordingly.

Column “3” shows the results of equalizing the maximum voltage levels at the *z*-terminals to 100mV for an input current of 1mA. For fixed capacitances, these levels are modified by the internal current gains *b* of CDTAs. Changing the *x*-terminal currents must be compensated by another modification of the transconductances. Due to changing the input currents of attenuators $K_{i,1}$ and $K_{i,3}$, their current transfers were also modified.

A final SPICE simulation of optimized filter has been performed. The corresponding SPICE model of the CDTA element [2] consists of two parts: The model of a current source I_z controlled by the difference of currents I_p and I_n is adopted from the model of CDBA element [10]. The transconductance amplifier is modelled by the SPICE model of the commercial 275MHz amplifier MAX435.

Current amplifiers/attenuators $K_{i,1}$ and $K_{i,3}$ were implemented by a cascade of two active current dividers with two CDTA elements [3]. Due to input resistances/capacitances of 2Ω/1pF of the *p*- and *n*-terminals of CDTA, capacitors C_2 and C_4 in Fig. 3 are not properly grounded, which causes undesired modifications of the frequency response. That is why we have implemented CDTAs No 1 and 3 as three-output devices [11] and the additional *x*-outputs were led directly into the inputs of active current dividers. Then C_2 and C_4 were normally grounded. The final results of SPICE simulation are in Fig. 5.

6 Conclusion

The above filter structure, based on the simulation of an arbitrary transfer function by a generalized current divider, is implemented by CDTAs and capacitors.

Transconductances and working capacitances can easily be designed directly from the denominator coefficients of the transfer function. Some possible ways of subsequent filter optimization are also described. This optimization is effective in combination with computer simulation, with the utilization of CDTA models [2], [9].

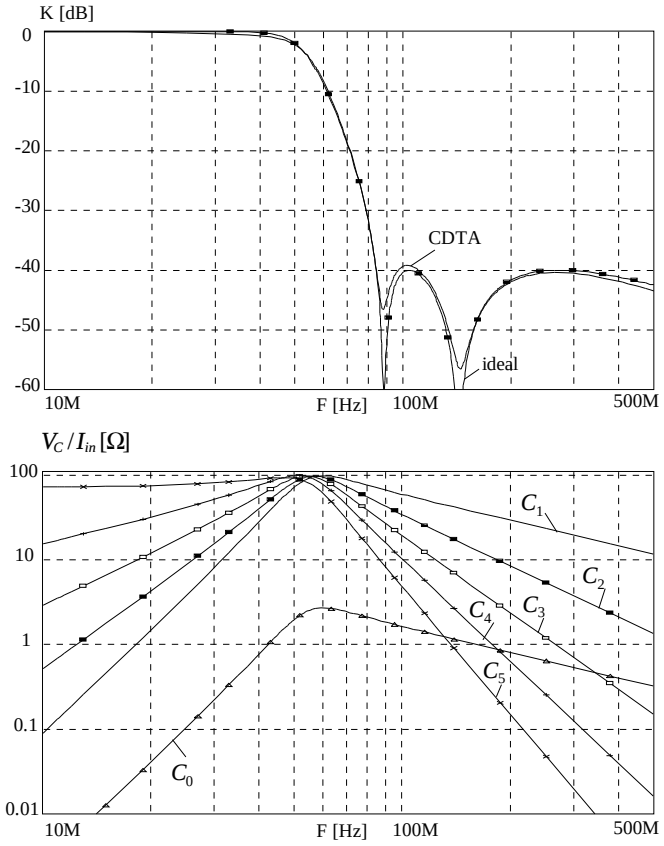

Fig. 5: SPICE simulation of the optimized filter in Fig. 3. Component values are in column "3" of Table 2.

Hitherto performed simulations offer satisfactory results for working frequencies of about hundreds of MHz.

Acknowledgments

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