Switched Realization of Nonrecursive Discrete Linear-Phase FIR Filters

Dalibor BIOLEK* Karel ZAPLATÍLEK*

Abstract

An unconventional method of exactly linear-phase filter design for analog signal processing is presented in this paper. The filters are designed by means of the discrete-time (DT) linear phase FIR prototypes. The resulting filter is constructed as a chain of unified switched blocks.

1. Introduction

The *N*-th order DT FIR filter with impulse response coefficients a_k can be described by its *z*-domain system function

$$H(z)=\sum_{k=0}^{N} a_{N-k} z^{-k} . \qquad (1)$$

In case of the well-known impulse response symmetry or asymmetry [1], [2]

$$a_k = a_{N-k} \text{ or } a_k = -a_{N-k}, \; k = 0,1,..,N , \qquad (2)$$

the group delay is exactly constant. The realization of a switched-capacitor filter with the same *z*-domain system function yields the linear-phase filter for analog signal processing.

2. Proposed switched building blocks

The basic building blocks are introduced in Fig. 1a,b, and the corresponding switching diagram in Fig. 1c. As shown below, the cascade connection of *N*+1 such blocks realizes the *N*-th order FIR filter. Thus each block realizes one coefficient a_k. In case it is necessary to have a negative coefficient, the A and B outlets must be interchanged (to ground outlet A, and to connect outlet B to input *x*).

Let us analyze the *i*-th block of type 1. The following equations are true:

$$d_i(kT+T_1)=v_i(kT+T_1), \qquad (3)$$

$$d_i(kT+T)=d_i(kT+T_1)+a_i x_i(kT+T_1). \qquad (4)$$

Due to possible signal discontinuities, the formulas of DT signals in equations (3) and (4) have to be understood as left-side limits.

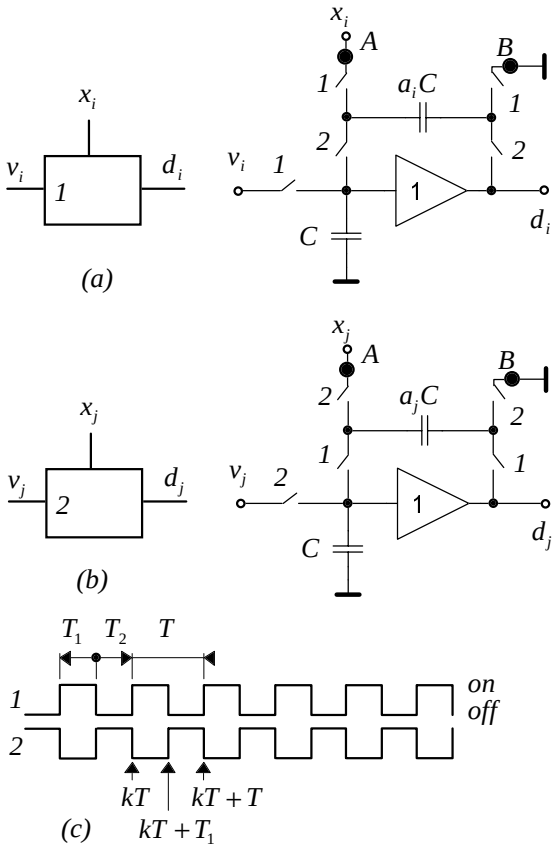

Fig. 1. Switched building blocks for cascade FIR synthesis: (a) type1, (b) type 2, (c) switching diagram.

Apply so-called Z_ε transform [3], [4]

$$\tilde{D}(z,\varepsilon)=\sum_{k=-\infty}^{\infty} d(kT+\varepsilon T) z^{-(k+\varepsilon)}, k \in \langle 0,1) \qquad (5)$$

to (3) and (4). In contrast to the classical *Z* transform, the Z_ε one preserves the phase spectral properties of

*Department of Electrical Engineering, Brno Military Academy, Czech Republic

discrete signals. We introduce the following notation:

$$\tilde{D}^1 = \sum_{k=-\infty}^{\infty} d(kT + T_1) z^{-(k+\varepsilon_1)}, \varepsilon_1 = T_1/T\,, \quad (6)$$

$$\tilde{D}^2 = \sum_{k=-\infty}^{\infty} d(kT) z^{-k}\,, \quad (7)$$

where $\tilde{D}^1 / \tilde{D}^2$ are Z_ε transforms of so-called equivalent signals in the phases 1/2 [4], [5]. Applying Z_ε transform to (3) and (4) yields

$$\tilde{D}_i^1 = \tilde{V}_i^1, \quad (8)$$

$$\tilde{D}_i^2 = \tilde{D}_i^1 z^{-\varepsilon_2} + a_i \tilde{X}_i^1 z^{-\varepsilon_2}, \varepsilon_2 = T_2/T\,. \quad (9)$$

Similarly, the *j*-th block of type 2 can be described by equations

$$d_j(kT + T_1) = d_j(kT) + a_j x_j(kT), \quad (10)$$

$$d_j(kT) = v_j(kT). \quad (11)$$

After Z_ε transform

$$\tilde{D}_j^1 = \tilde{D}_j^2 z^{-\varepsilon_1} + a_j \tilde{X}_j^2 z^{-\varepsilon_1}, \quad (12)$$

$$\tilde{D}_j^2 = \tilde{V}_j^2\,. \quad (13)$$

3. Synthesis using signal flow graphs

Consider a chain of basic building blocks according to Fig. 2. The blocks of type 1 and 2 change their order in the cascade. *x* is the input signal of the FIR filter. The filter output corresponds to the d_N output of the last block.

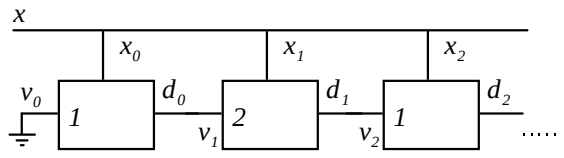

Fig. 2. Cascade of basic switched blocks.

After applying equations (8), (9), (12) and (13), the cascade structure in Fig. 2 can be modelled by using the signal flow graph in Fig. 3.

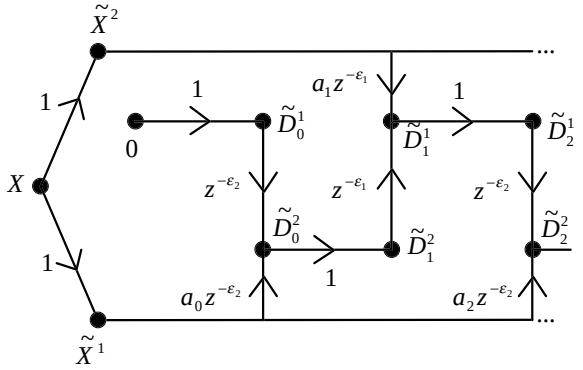

Fig. 3. Signal flow graph of the cascade in Fig. 2.

The following simplifications were used for the graph design:

1. An identical signal is taken to *x*-inputs of all blocks. Thus the subscripts can be omitted.
2. If input signal *x* fulfills the condition of the Nyquist sampling theorem, then it is identical to its equivalent signals [4]:

$$\tilde{X}^1 = \tilde{X}^2 = X\,. \quad (14)$$

In the following considerations, we confine ourselves to the applications with identical lengths of switching phases, i.e.

$$T_1 = T_2 = T/2\,. \quad (15)$$

We introduce a simplifying notation

$$w = z^{1/2} = z^{\varepsilon_1} = z^{\varepsilon_2} = e^{j\omega T/2}\,. \quad (16)$$

Under the given conditions, the graph in Fig. 3 can be further simplified. Its evaluation produces a system function for the output sample selection in phases 1 and 2. The results depend on whether *N* is even or odd.

<u>*N* odd:</u>

$$K^1 = \frac{\tilde{D}_N^1}{X} = w^{-1} \sum_{k=0}^{N} a_{N-k} w^{-k}\,, \quad (17)$$

$$K^2 = \frac{\tilde{D}_N^2}{X} = w^{-1} \sum_{k=0}^{N-1} a_{N-k-1} w^{-k}\,. \quad (18)$$

<u>*N* even:</u>

$$K^1 = \frac{\tilde{D}_N^1}{X} = w^{-1} \sum_{k=0}^{N-1} a_{N-k-1} w^{-k}\,, \quad (19)$$

$$K^2 = \frac{\tilde{D}_N^2}{X} = w^{-1} \sum_{k=0}^{N} a_{N-k} w^{-k}\,. \quad (20)$$

It should be noted that the system functions for output phase 1, N odd, and for output phase 2, N even, are of the *N*-th order, while the remaining ones are only of the *N*-1 order. Only equations (17) and (20) correspond to the N-th order FIR filter. That is why it is necessary to put a proper circuit of the sample selection (e.g. Sample-Hold) between the output of the N-th block and the output of the whole filter.

Comparing equations (1) and (17) or (20) results in two partial conclusions:

1. The symbol *z* in (1) is replaced by symbol *w*. Taking into account equation (16), the filter described by (17) or (20) behaves as a DT filter with the actual double sampling frequency 2*1/T. This fact has to be considered during the z-domain filter synthesis.
2. An additional symbol w^{-1} in (17) and (20) refers to the additional delay of the output signal by the time interval T/2, which does not violate the group delay to be constant.

4. Real properties

For practical realization, the following main real properties affect the filter behavior:

Analog switches:

1. Nonzero *R*-on switch resistances.
2. Nonzero t_{ON} and t_{OFF} switching times.
3. Logical feedthrough.

Unity-gain buffers:

1. Finite Gain-Bandwidth product (*GBW*).
2. Nonzero output resistance
3. Not exactly unity DC amplification.

Nonzero *R*-on switch resistances.

Due to nonzero *R*-on switch resistances, the capacitors are charged and discharged with a certain nonzero time constants. This causes some imperfections in the filter behaviour if these time constants are comparable to the duration of switching phases T_1 and T_2.

Let us demonstrate this influence for the block of type 1. There are four types of *R*-on influences:

1. An additional *z*-domain pole

$$z = e^{-T_1/\tau_1}$$

for each block, where $\tau_1 = R_{ON} C$ is a time constant of charging capacitor *C* from voltage input *v*.

To preserve constant group delay, it is essential to keep ratio T_1/τ_1 as large as possible.

2. The *a* coefficient is modified according to the equation

$$a \to a\left(1 - e^{-T_2/\tau_2}\right),$$

where τ_2 is a time constant of discharging capacitor *aC* across the buffer terminals.

That is why it is necessary to keep ratio T_2/τ_2 as large as possible.

3. Additional coefficients of transfer function appear due to nonzero R_{ON} and the filter order increases. These coefficients are proportional to the value

$$a\, e^{-T_1/\tau_1}\left(1 - e^{-T_2/\tau_2}\right)$$

and modify the ideal group delay response. To prevent it, the recommendation is the same in the item 1.

4. An additional *s*-domain pole

$$s = \frac{1}{aCR_x}$$

appears due to charging capacitor *aC* from input *X* through the series resistance R_X which is created by the *R*-on resistances of two switches in series. It is necessary to keep this pole outside the region of working frequencies.

Nonzero t_{ON} and t_{OFF} switching times.

The dynamic behavior of analog switches limit maximum switching frequency. For our experiments, we used MAX4521 Rail-to-Rail switches with the typical values

$$t_{on} \approx 45\text{ns}, t_{off} \approx 15\text{ns}.$$

Then the maximum switching frequency does not reach the value

$$\frac{1}{2\left(t_{on} + t_{off}\right)} \doteq 8.3\text{MHz}\cdot$$

It should be noted that due to the property (16), the switching frequency 8 MHz means the actual frequency 16 MHz of the designed discrete-time filter.

Logical feedthrough

is the well-known phenomenon connected with the utilization of analog switches. It can be partially eliminated by using charge-balanced switching structures.

Real properties of buffer.

The buffer finite *GBW* along with its nonzero output resistance R_0 and DC gain not precisely equal to one can lead to interesting influences whose discussion is beyond the scope of this contribution. A sufficiently high *GBW* produces slight modification of the coefficient *a* and generates additional high-order coefficients. A rough rule of thumb is as follows:

$$GBW > 50\, f_{SAMPLING} \quad (21)$$

$$R_0 < R_{ON}/10. \quad (22)$$

In our experiments, we used BUF600 with *GBW*=320MHz (for 5V p-p) and output resistance 6Ω. According to the (21) and (22), the sampling frequency would not exceed the value 6 MHz and the R0 influence would not be important for switch resistance above 60Ω.

5. Experimental verification of the principle

Consider an analog filter with an amplitude frequency response which is specified by the tolerance diagram in Fig. 4. In the first step, we designed the 4-th order DT linear-phase FIR filter by using the Chebychev windowing with the following parameters:

- sampling frequency 100 kHz
- coefficients according to the Table 1.

Then we synthetized this FIR filter using the cascade switched structure in Fig. 2. To realize 5 coefficients from the Table 1, we used 5 switched blocks (3 blocks of type 1, 2 blocks of type 2).

Together with one switch for output sample selection, we needed 26 analog switches which were realized using 7 quad MAX 4521 circuits with R_{ON} < 100Ω. According to the condition (16), the real switching frequency was used 50 kHz.

For basic capacitances C=1nF, all the conditions given in the part "*Real properties*" are fulfilled.

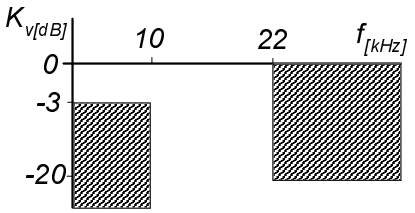

Fig. 4. Tolerance diagram of designed filter.

Table 1: Coefficients of designed DF linear-phase filter that matches the tolerance diagram in Fig. 4.

a_0	0.13730940277985
a_1	0.22596280162128
a_2	0.27345559119773
a_3	0.22596280162128
a_4	0.13730940277985

Measuring magnitude frequency response and group delay using the HP 4195A 10 Hz-10MHz circuit analyzer confirmed our design requirements.

6. Conclusion

This paper proposes a simple method of construction cascade switched filter for analog signal processing with the principally linear phase response. Due to unified switched blocks in the cascade, this solution would be suitable for integrated realization. Then it would enable to reach sufficiently high order, which is necessary for FIR structures.

Acknowledgement

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