Current-Mode CDTA-Based Comparators

Dalibor Biolek, Viera Biolková*)

Dept. of Microelectronics/Radioelectronics, FEEC, Brno University of Technology, Czech Republic

fax 973442987- e-mail dalibor.biolek@unob.cz- http://user.unob.cz/biolek

Abstract

The paper explains basic ideas how to construct current-mode comparators with the utilization of CDTA (Current Differencing Transconductance Amplifier) active circuit elements. These comparators enable fast comparison of input currents including a prospective hysteresis. Basic application in the area of current-mode signal generation is described. SPICE simulations are provided, based on CMOS-level SPICE modeling of the CDTA.

1 Introduction

The active circuit component CDTA (Current Differencing Transconductance Amplifier) is particularly useful for the current-mode applications, because its input and output signals are currents [1]. CDTA consists of the input current-differencing unit and of multiple-output OTA (Operational Transconductance Amplifier). Its block oriented structure is similar to the CDBA element (Current Differencing Buffered Amplifier) [2], in which the voltage unity-gain buffer is used instead of the OTA.

Till this time, a set of transistor structures of the CDTA element has been published, both in the CMOS [1-7] and bipolar [8, 9] technologies. The computer simulations predict the “faster” applications than for the CDBA element. Namely the linear applications from the area of frequency filtering are described in the literature: 2nd-order filters [1, 7-11], general multiple-feedback active filters [3, 4, 6], gyrators [12], allpass cells [12, 13], passive ladder structure simulations [14], etc. Oscillator circuits are also reported [15, 16].

Because of high current gain of the CDTA which is comparable to voltage gain of a classical voltage-feedback operational amplifier, the CDTA can be used as a current comparator. The required hysteresis can be accomplished by applying a proper positive feedback. In the paper, the behavior of the CDTA element in this nonlinear regime will be described as well as a demonstration of concrete application, i.e. rectangular wave generator.

2 Current comparator employing the CDTA element

A comparison of conventional voltage-mode Schmitt trigger (a) and current-mode CDTA-based trigger (b) is shown in Fig. 1. The CDTA element has a couple of low-impedance input terminals p and n. The difference of currents I_p and I_n flows out of the z terminal into an outside load, causing the voltage drop which is transferred to current I_x via the internal transconductance g_m. When the z terminal is not loaded, the voltage across this terminal is given by its high internal resistance. The product of this impedance and the transconductance g_m represents the current gain of the CDTA. Value of current I_x is limited by internal current source I_c, which is a part of the transconductance stage. When the product of the difference input current I_p-I_n and the current gain is beyond the interval $<-I_c, I_c>$, the current I_x will be clipped, analogous to the output voltage limitation of the operational amplifier in the saturation regime.

The hysteresis can be implemented in the comparator in Fig. 1 (b) by positive feedback using the current divider R_1-R_2, similarly as for conventional voltage-mode comparator in Fig. 1 (a), when the feedback signal is led from the voltage divider. A comparison of the hysteresis curves of both comparators is also given in the figure.
The simplest current-mode Schmitt trigger is provided after replacing R_1 by short connection and disconnecting R_2. Then the toggle levels of the input current will be $\pm I_c$.
Note that the hysteresis curve of the current comparator can be easily shifted along the horizontal axis by applying an auxiliary DC current to the *n* or *p* terminal.

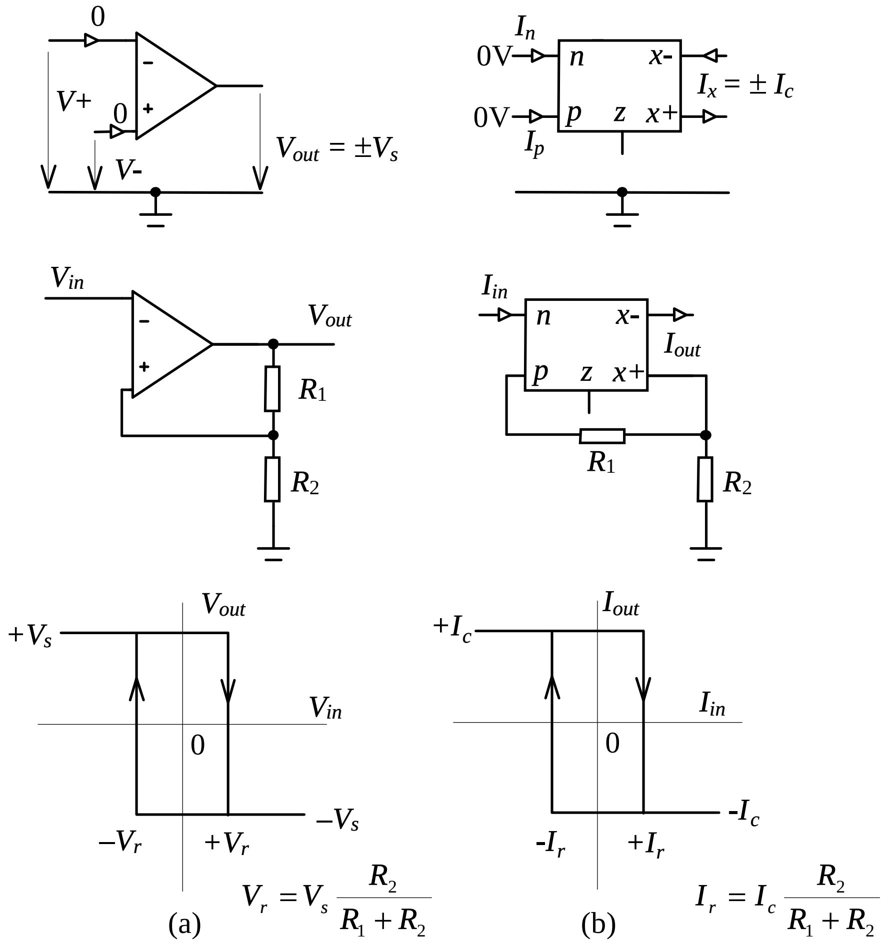

Fig. 1: Schmitt trigger employing (a) operational amplifier, (b) CDTA element.

3 Computer simulation

To verify the behavior of proposed comparator, PSpice simulation has been performed. The CDTA element has been modeled by a CMOS structure from [7, 15]. The transistor parameters were used from 0.5µ MIETEC technology. The indispensable parasitic resistances of *n* a *p* terminals of CDTA must be taken into account for this application. In the given topology, they represent values of 2kΩ and 7kΩ. Since the resistance of the *n* terminal is less than the resistance of the *p* terminal, the feedback has been led from the *x*- output into the *n* input, and the input current has been conveyed into the *p* terminal. During the comparator design, the internal resistance 2kΩ of the *n* terminal must be included to the value of R_1.
Fig. 2 shows the results of Transient analysis which has been performed with the aim to obtain the hysteresis curve of the comparator. This curve is plotted on the following assumptions: the input current I_{in} is a triangular waveform with the swing from -100µA to

+100μA. Its frequency is stated to 1Hz with the aim to avoid circuit dynamical transients during the simulation. The controlling current I_c is set to 50μA. The output *x*+ is loaded by a resistance R_L=1Ω. The resistor R_1 is replaced by short connection such that only the internal resistance 2kΩ of they *n* terminal is asserted. The resistance R_2 is set to 2kΩ, thus the comparator toggle levels should be ±25μA. These conclusions are fully in accordance with the simulation results in Fig. 2.

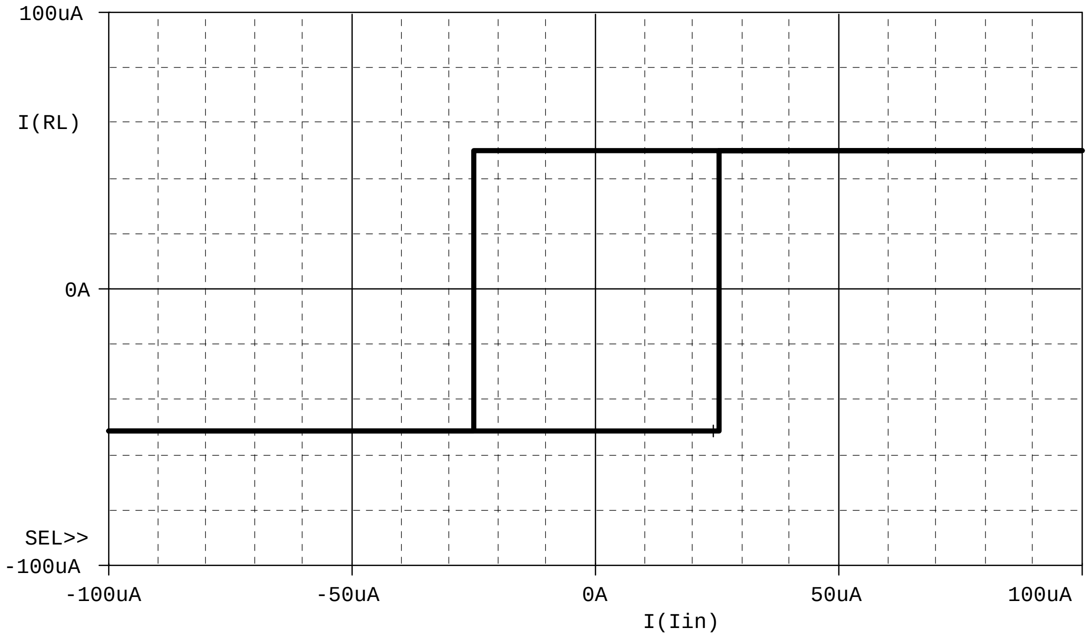

Fig. 2: Simulated hysteresis curve of the comparator.

Fig. 3 demonstrates a simulation of the propagation delay of the comparator. The hysteresis is removed by breaking the path between the ***x*-** and ***n*** terminals and removing R_2. The frequency of input current is now 5MHz. The propagation delay is 8.3ns for toggling from low to high level and 6ns from high to low level.

Fig. 3: Measuring the propagation delays.

4 Demonstration of the waveform generator

The proposed generator is in Fig. 4. Current comparator is completed by a frequency dependent current divider *R*-*C*, connected into the negative feedback loop. Results of PSpice simulation are in Fig. 5. This circuit can provide rectangular waveforms in the frequency band of tens of MHz.

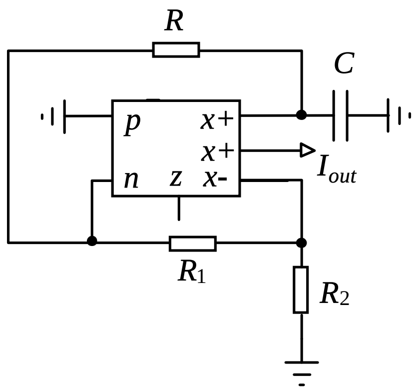

Fig. 4: Waveform generator employing CDTA element.

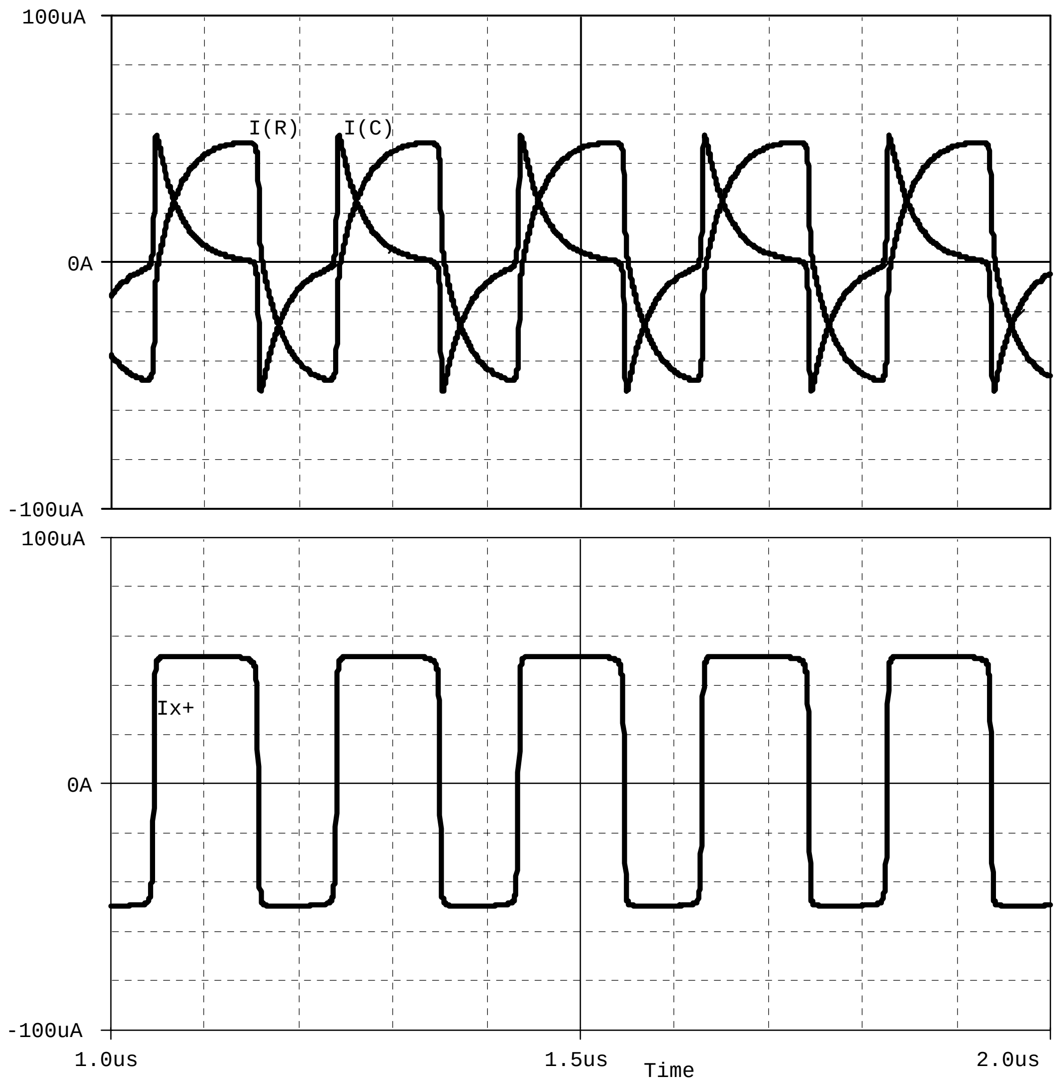

Fig. 5: Waveforms of circuit in Fig. 4. $R = 1.5\text{k}\Omega$, $C = 10\text{pF}$. Repeating frequency is 5.2MHz.

5 Conclusions

A possibility of implementation of current comparators employing the CDTA elements is reported in the paper. These comparators can be used in current-mode applications which exhibit dual properties to the commonly used voltage-mode circuits. Computer simulations have been performed with the utilization of CDTA model in 0.5μm CMOS technology. Modeling of simple current-mode waveform generator demonstrates its proper operation in the frequency region of tens of MHz. One can expect further increase of the speed of such CDTA applications after passing to 0.35μm or more advanced technology.

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