FLOATING GIC AND ITS IMPLEMENTATION

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ABSTRACT:

A novel Generalized Impedance Converter (GIC) is described in the paper. The circuit consists of a pair of 2nd generation current conveyors and one voltage follower. A floating impedance Z_1 and two grounded impedances Z_2 and Z_3 are transformed into the input impedance according to the formula $Z_{in} = Z_1*Z_3/Z_2$. The circuit principle is verified via computer simulation.

Keywords: GIC, FDNR, floating inductor, current conveyor

1 INTRODUCTION

Replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design. An efficient way of simulating the floating inductor consists in replacing the inductor by three OTAs (Operational Transconductance Amplifier) and one grounded capacitor [1]. However, the common drawback of OTAs is the low-level input voltage providing the linear mode of the amplifier. This can be in conflict with the requirements for a large dynamic range of signals being processed. When the filter is designed for the current-mode, the current limitations of the active elements should also be carefully monitored.

Impedance converters find application particularly in active filters, where they simulate circuit elements which are hard to integrate on a chip (especially inductors), or which must be set up artificially (e.g. Frequency Dependent Negative Resistors – FDNRs).

A study of the existing publications about impedance converters, e.g. [1, 2] and the papers referenced herein, leads to the conclusions summarized below:

A Generalized Impedance Converter (GIC) consists of *NA* active circuit elements and *NP* passive impedances Z_k, k = 1, 2, … *NP*, where *NP* is (with only a few exceptions) an odd number. The input impedance of the converter is given as follows:

$$Z_{in} = \pm \frac{Z_1}{Z_2} \frac{Z_3}{Z_4} \ldots \frac{Z_{NP-2}}{Z_{NP-1}} Z_{NP} . \qquad (1)$$

The positive/negative sign in (1) appertains to the positive/negative impedance converter. The input terminals, between which the impedance is measured, can be either floating or one of them is grounded.

Such devices are frequently used to simulate inductors (one of the impedances in the denominator is of capacitive character), floating capacitors based on grounded capacitors (one of the impedances in the numerator is of capacitive character), FDNRs (two impedances in the numerator are of capacitive character), or the so-called high-order immitances (more impedances in the numerator/denominator have a capacitive character). Then the minimum

possible number of passive elements *NP* is 3, 1, or 3 in the first, second and third case, respectively.

Formerly utilized operational amplifiers (OpAmps) are currently replaced by other active elements. One reason is the fact that in some cases the OpAmp-based impedance converters have a rather complicated topology and that their operation is based on fulfilling several relations among the parameters of passive elements. From this point of view, current conveyors, particularly CCII+ or CCII-, appear to be more advantageous active elements for implementing the impedance converters [1].

In addition to the right-side impedances in Eq. (1), the ubiquitous parasitic impedances impact the circuit behavior and modify the equation for the input impedance. The results of the analysis of such modifications are often critical in selecting such circuit implementations of impedance converters which are suitable for a concrete application.

The paper deals with a positive impedance converter with floating input terminals and with *NP*=3, which is potentially useful for the simulation of floating and grounded inductors, capacitors, and FDNRs. In [2], such converters are described which employ four CCII+ or CCII- and three impedances. An economical circuit employing only two current conveyors is given in [3]. However, this circuit requires several external passive elements and their parameters must fulfill exact matching conditions. The sensitivities of the input impedance to the parameters of these elements are then high. An interesting low-sensitive impedance converter with a pair of CCII- and *NP*=5 is proposed in [4] with the input impedance according to (1).

In this paper, a novel implementation of floating positive impedance converter is described. It consists of three impedances, one CCII+, one CCII±, and one voltage buffer. The choice of such active elements was partially motivated by their easy implementation using commercially integrated circuits. Active elements such as CCII+ and buffer are directly available as OPA860 [5]. The CCII- can be compiled from two CCII+ [2].

2 PROPOSED IMPEDANCE CONVERTER

The proposed impedance converter is shown in Fig. 1 (a).

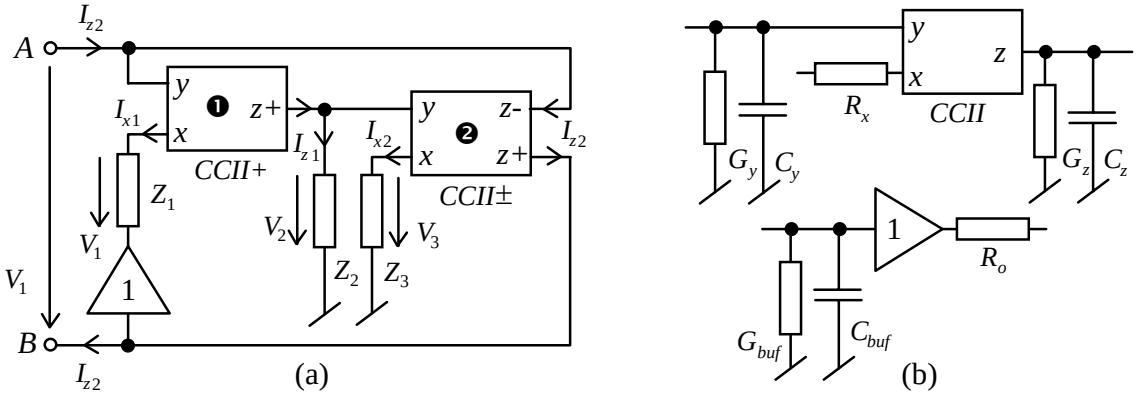

Fig. 1: (a) proposed impedance converter, (b) parasitic impedances, affecting the converter operation.

In the first step, let us assume that active elements of the converter are ideal. Then voltage V_1 between the *A*-*B* terminals appears at the impedance Z_1 and affects current $I_{x1} = V_1/Z_1$. This current also flows out of the *z*+ outlet as I_{z+}, causing a voltage drop at Z_2, namely $V_2 = Z_2\, I_{Z1} = V_1\, Z_2/Z_1$. This voltage is equal to voltage V_3. Thus, the currents I_{x2} and I_{z2} are

$$I_{x2} = I_{z2} = \frac{V_3}{Z_3} = \frac{Z_2}{Z_1 Z_3} V_1 .$$

These currents are also the terminal currents. The input impedance will be as follows:

$$Z_{in} = \frac{V_1}{I_{z2}} = \frac{Z_1}{Z_2} Z_3 = Z_1 Y_2 Z_3 . \tag{2}$$

Comparing equations (2) and (1), one can conclude that in the ideal case, the circuit in Fig. 1 (a) behaves as a positive impedance converter with $NP = 3$.

3 ANALYSIS OF THE INFLUENCE OF PARASITIC IMPEDANCES

3.1 Alternative model of impedance converter

The dominant parasitic impedances of CCII and voltage buffer are shown in Fig. 1 (b): both the buffer input impedance and the impedance of *y* and *z* terminals of the conveyor are of capacitive character. In the low-frequency region, the output impedances of the buffer and the *x* terminal of the conveyor are resistive. When the frequency increases above a certain limit, which is given by the active device parameters, the inductive part of the impedance appears. Simple modeling in Fig. 1 (b) is accurate enough within a frequency band of up to circa tens or hundreds of MHz. Let us suppose that no other influences, such as frequency dependence of the buffer gain, will play a role in the working frequency region.

Specifically, the following parasitic parameters are mentioned in [5] for the OPA860 integrated circuit:

$$\begin{aligned} &R_y = 455\text{k}\Omega \Rightarrow G_y = 2.2\mu\text{s},\ C_y = 2.1\text{pF},\ R_z = 54\text{k}\Omega \Rightarrow G_z = 18.5\mu\text{s},\ C_z = 2\text{pF}, \\ &R_{buf} = 1\text{M}\Omega \Rightarrow G_{buf} = 1\mu\text{s},\ C_{buf} = 2.1\text{pF},\ R_O = 1.4\Omega,\ R_x \geq 10.5\Omega. \end{aligned} \tag{3}$$

The last specification is based on the fact that resistance R_x is inversely proportional to transconductance g_m, which can be adjusted electronically for OPA860. The highest value of g_m is approximately 95mA/V [5], which corresponds to the lowest value of R_x given above.

An analysis of the circuit in Fig 1 (a) shows the following consequences of the influence of parasitic elements (3) on the model of impedance converter:

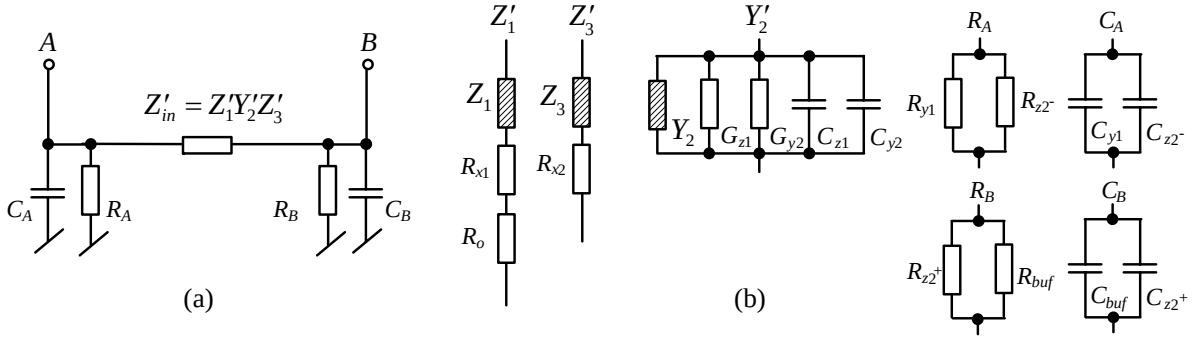

Fig. 2: Model of the impedance converter from Fig. 1, with real effects taken into consideration. The hatched impedances in Fig. (b) are working, the remaining are parasitic.

Parasitic shunt resistance R_A (R_B) and parasitic shunt capacitance C_A (C_B) act between the *A* (*B*) terminals and the ground. The parameters R_A, C_A, R_B, and C_B depend on the parasitic impedances of active elements according to Fig. 2 (b). Considering the nominal values for OPA860 according to (3), we get

$$\begin{aligned} &R_A = R_{y1} \,\&\, R_{z2}\text{-} \approx 48.3\text{k}\Omega,\ C_A = C_{y1} + C_{z2}\text{-} \approx 4.1\text{pF}, \\ &R_B = R_{z2}\text{+} \,\&\, R_{buf} \approx 51.2\text{k}\Omega,\ C_B = C_{buf} + C_{z2}\text{+} \approx 4.1\text{pF}. \end{aligned} \tag{4}$$

Such parasitic values should be taken into account when designing concrete applications of the impedance converter.

For the impedance between the *A*-*B* terminals, formula (2) is still true, but individual impedances on the right-side of the equation are modified by the parasitic impedances according to Fig. 2 (b). An analysis of these modifications is provided in the next Sections for three concrete types of application of the impedance converter.

3.2 Simulation of floating inductor

The impedance converter will simulate the floating inductor on the following assumptions:

$$Z_1 = R_1,\ Y_2 = sC_2,\ Z_3 = R_3. \tag{5}$$

Eq. (2) then leads to the result

$$Z_{in} = sL,\ L = R_1 R_3 C_2. \tag{6}$$

The parasitic impedances (see Fig. 2) will modify the input impedance as follows:

$$Z'_{in} = Z'_1 Y'_2 Z'_3 = (R_1 + R_{x1} + R_o)(sC_2 + G_{z1} + G_{y2} + sC_{z1} + sC_{y2})(R_3 + R_{x2}).$$

After a small arrangement we get

$$Z'_{in} = R' + sL', \text{ where} \tag{7}$$

$$R' = (R_1 + R_{x1} + R_o)(R_3 + R_{x2})(G_{z1} + G_{y2}),\ L' = (R_1 + R_{x1} + R_o)(R_3 + R_{x2})(C + C_{z1} + C_{y2}). \tag{8}$$

The parasitic impedances cause a modification of simulated inductance. In addition, a series lossy resistance *R*‘ appears. The ratio of the imaginary to the real part of impedance (7) is

$$\frac{\omega L'}{R'} = \omega \frac{C + C_{z1} + C_{y2}}{G_{z1} + G_{y2}}. \tag{9}$$

Ratio (9) is the inductor quality factor, or the reciprocal value of the tan(δ) at the frequency ω. To maximize it during the inductor design while simultaneously respecting concrete parasitic impedances, we should maximize the working capacitance C_2 and minimize the resistances R_1 and R_3. From this point of view, the working resistors should be designed as short circuits. Then the parasitic resistances would substitute their role. This seems to be unpractical due to the direct dependence of the simulated inductance on the parasitic elements. However, an interesting possibility appears when using integrated circuits such as OPA860, where the resistance of the *x* terminal can be electronically set to a defined value. Then the above conditions R_1=0, R_3=0 can be used for a consistent optimization.

3.3 Simulation of floating capacitor

The simulation of the floating capacitor whose capacitance is derived from the capacitance of another grounded capacitor is feasible on the assumption that

$$Z_1 = R_1,\ Y_2 = G_2 = \frac{1}{R_2},\ Z_3 = \frac{1}{sC_3}. \tag{10}$$

Then

$$Z_{in} = \frac{1}{sC},\ C = C_3 \frac{R_2}{R_1}. \tag{11}$$

Considering the influence of the parasitic impedances according to Fig. 2 (b), we obtain a modified input impedance

$$Z'_{in} = R' + sL' + \frac{1}{sC'}, \tag{12}$$

where
$$R' = (R_1 + R_{x1} + R_0)\left[\frac{C_{z1} + C_{y2}}{C_3} + R_{x2}(G_2 + G_{y1} + G_{y2})\right],$$
$$L' = (R_1 + R_{x1} + R_o)R_{x2}(C_{z1} + C_{y2}), \tag{13}$$
$$C' = \frac{C_3}{(R_1 + R_{x1} + R_o)(G_2 + G_{z1} + G_{y2})}.$$

Note that a parasitic resistor and a parasitic inductor appear in series with the simulated capacitor. A simple computation reveals the values of resonant frequency ω_r and quality factor Q of the corresponding series resonance tank:

$$\omega_r = \sqrt{\frac{G_2 + G_{z1} + G_{y2}}{R_{x2}C_3(C_{z1} + C_{y2})}},\ Q = \frac{\sqrt{\alpha}}{1+\alpha}, \text{ where } \alpha = \frac{C_{z1} + C_{y2}}{R_{x2}C_3(G_2 + G_{z1} + G_{y2})}. \tag{14}$$

An analysis shows that the quality factor cannot be greater than 0.5 in any case. In other words, the circuit is well damped. Throughout the converter design, the C_3 and G_2 parameters should be chosen such that they shift the resonant frequency sufficiently beyond the working frequency region of a given application.

3.4 Simulation of the FDNR

Theoretically, the ideal FDNR can be simulated using the impedance converter in Fig 1 (a) under the following conditions:

$$Z_1 = \frac{1}{sC_1},\ Y_2 = G_2 = \frac{1}{R_2},\ Z_3 = \frac{1}{sC_3}. \tag{15}$$

Then
$$Z_{in} = \frac{1}{s^2 D},\ D = R_2C_1C_3. \tag{16}$$

The influence of the parasitic impedances causes the modified result

$$Z'_{in} = R' + sL' + \frac{1}{sC'} + \frac{1}{s^2 D'}, \tag{17}$$

where $R' = (C_{z1} + C_{y2})\left(\frac{R_{x1} + R_o}{C_3} + \frac{R_{x2}}{C_1}\right) + R_{x2}(R_{x1} + R_o)(G_2 + G_{z1} + G_{y2}),$

$$L' = (R_{x1} + R_o)R_{x2}(C_{z1} + C_{y2}), \tag{18}$$
$$1/C' = \frac{C_{z1} + C_{y2}}{C_1C_3} + (G_2 + G_{z1} + G_{y2})\left(\frac{R_{x1} + R_o}{C_3} + \frac{R_{x2}}{C_1}\right),\ D' = \frac{C_1C_3}{G_2 + G_{z1} + G_{y2}}.$$

In reality, the value of D is modified, and there also appears a lossy resonant circuit in series with the FDNR. An analysis of the consequences of this fact is beyond the scope of this paper.

4 DESIGN EXAMPLE

As an example, let us design a floating capacitor with C = 10nF on the basis of a grounded capacitor with the capacitance C_3 = 100pF. A design rule $R_2 = 100R_1$ results from Eq. (11) which is true for an ideal case without any parasitic impedances of active elements being taken into consideration.

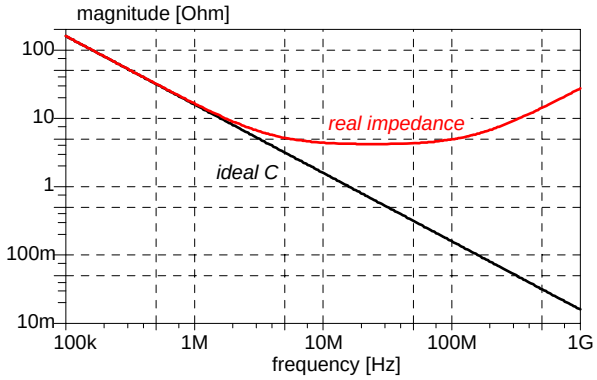

Fig. 3: Computer simulation of the frequency dependence of the impedance of the synthetic floating capacitor.

Consider current conveyors with the parameters of OPA860 circuits according to (3). The *x*-resistance of CCII No. 1 will be set to 98.6Ω. Together with the buffer output resistance R_o, it forms the resistance R_1 = 100Ω. The resulting resistance will be weakly dependent on the value of parasitic resistance R_o. The resistance R_2 will be designed such that it creates, together with parasitic resistances R_{Z1} and R_{Y2}, a hundredfold of R_1, i.e. 10kΩ. A simple calculation leads to the value 12.6kΩ. The resistance R_{x2} should be selected as small as possible, i.e. 10.5Ω, since it operates in series with the working capacitor and decreases its quality factor.

A computer simulation of the frequency dependence of the *A*-*B* impedance has been performed using the SNAP program [6] with the result given in Fig. 3. A curve for the ideal capacitor with *C* = 10nF is added for comparison. There is good agreement up to ca. 2MHz. Then the influence of the series resistance *R*‘ (see Eq. 12 or 13) shows up, and the parasitic inductance starts increasing the impedance from frequencies exceeding ca. 100MHz.

5 CONCLUSIONS

The positive impedance converter described has the following features: (i) Two current conveyors CCII and one voltage buffer are the only required active elements, (ii) two of three internal impedances are grounded, (iii) all the active elements are available as commercial integrated circuits. In addition, note that the negative impedance converter can be easily obtained from the positive one by merely interchanging the current outputs of the CCII No. 2. An impedance converter for simulating the grounded, not the floating impedance originates from the circuit either by grounding the *A* terminal and omitting the *z*- terminal of CCII No. 2, or by grounding the *B* terminal, omitting the *z*+ terminal of CCII No. 2, and replacing the buffer by a short circuit.

6 ACKNOWLEDGMENT

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7 REFERENCES

[1] Schaumann R., Ghausi M. S., Laker K. R.; *Design of analog filters*. Prentice Hall, 1990.
[2] Lidgey J., Toumazou C.; *Current-Conveyor Basics and Applications*. Chapter 11.1 in the book Circuits&Systems. Tutorials, IEEE ISCAS’94, pp. 569-587.
[3] Wilson B.; *Recent developments in current-conveyors and current-mode circuits*. IEE Proc., Pt. G. 137 (2), 1990, pp. 63-77.
[4] Senani R.; *Floating ideal FDNR using only two current conveyors*. Electron. Lett., 20 (5), 1984, pp. 205- 206.
[5] OPA860. *Wide Bandwidth Operational Transconductance Amplifier (OTA) and Buffer*. Datasheet, Texas Instruments, SBOS331B, June 2006.
[6] Biolek D.; *SNAP - Program with Symbolic Core for Educational Purposes*. CSCC'00 Vouliagmeni, Athens, 2000, pp. 1711-1714.