# A LOW POWER DISSIPATION TECHNIQUE FOR CCII

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ABSTRACT:

Recently reducing the voltage supply and the power consumption of analog integrated circuits becomes an important design criteria especially in the environment of portable systems where a low supply voltage, given by a single cell battery, is used. In current mode approach the current conveyer (CCII) can be considered as a basic circuit block because all the active devices can be made of a suitable connection of one or two CCIIs [1].

## 1 ENHANCED BULK-DRIVEN CURRENT MIRROR PRINCIPLE

The main drawback of the bulk-driven current mirror introduced in [2] is the absence of the input-output current linearity, since the output transistor M2 is operating in saturation [2,5]. To solve this problem it can be used an alternative configuration (see Fig. 1). The transistor M3 is connected as a diode between the gate and the bulk terminal of both transistors M1, M2 and it is a simple realization of the voltage source [4,5]. When the input current Iin is zero the transistor M2 works in saturation and transistor M1 doesn't. As soon as the input current starts increasing, the transistor M1 in the enhanced bulk-driven reach the saturation earlier than the M1 in simple bulk-driven current mirror and therefore it has better linearity. Since this connection allow to drive both terminals the gate and the bulk at the same time. The current Ibias through M3 is added to Iin, and therefore Ibias has to be much smaller than Iin to avoid extra offset between Iin and Iout.

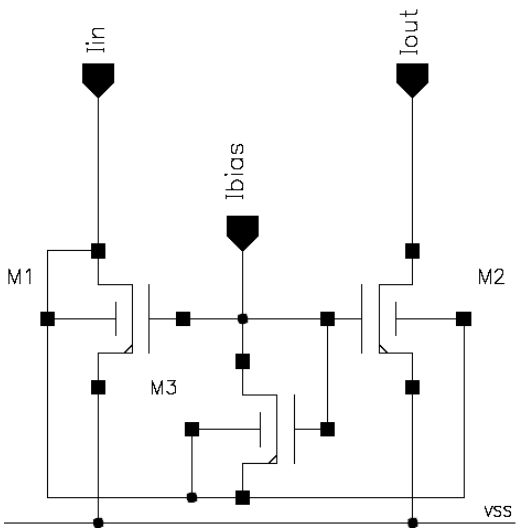


**Fig. 1**: Enhanced bulk-driven current mirror

The simulation result of the input-output transfer characteristics of enhanced bulk-driven current mirror shows better linearity than simple bulk-driven current mirror, this linearity is almost the same as the gate-driven current mirror.

## 2 A LOW POWER DISSIPATION TECHNIQUE FOR CCII

Fig. 2 shows current conveyor based on a single stage complementary source follower where the gate-source voltage VGS of two NMOS transistors (M1-M3) and two PMOS (M2-M4) are supposed to match, the input voltage VY is transferred to the output voltage VX of the follower precisely. The current mirrors (M5-M6) and (M7-M8) are transferring the current from the X terminals of the current conveyors to their Z terminals [1,3]. The enhanced bulk-driven technique has been used to remove the limitation of the conventional design [2,4]. The circuit has six additional transistors (M13, M14, M15, M16, M17 and M18) connected as a diode between the gate and the bulk terminal of transistors pair (M1-M3), (M2-M4), (M5-M6), (M7-M8), (M9-M10) and (M11-M12) respectively, actually this connection is a simple realization of the voltage source which allows driving both terminals the gate and the bulk of the transistor at the same time. The designs were simulated in Cadence using (I2T100) process which is a 0.7 µm CMOS twin tub technology from the AMI Semiconductor. The supply voltages are only ±0.5 V.

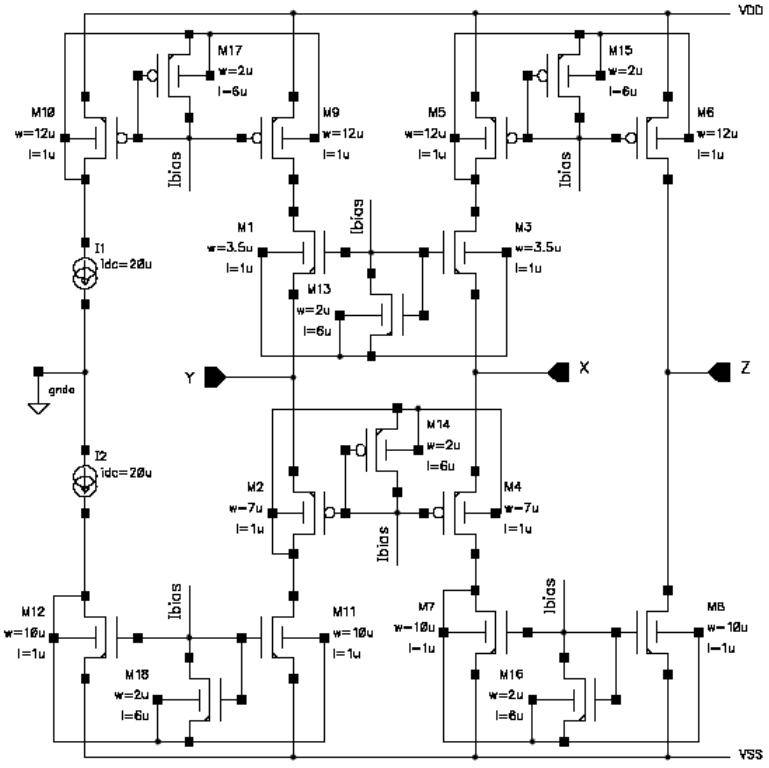


**Fig 2**: Enhanced bulk-driven current conveyor CCII

The current transfer ratio iz/ix in dB of the LV LP CCII is 1.1 and the 3dB Bandwidth is 65 MHz as show Fig. 3, which is quite high comparing to conventional LV LP CCII design.

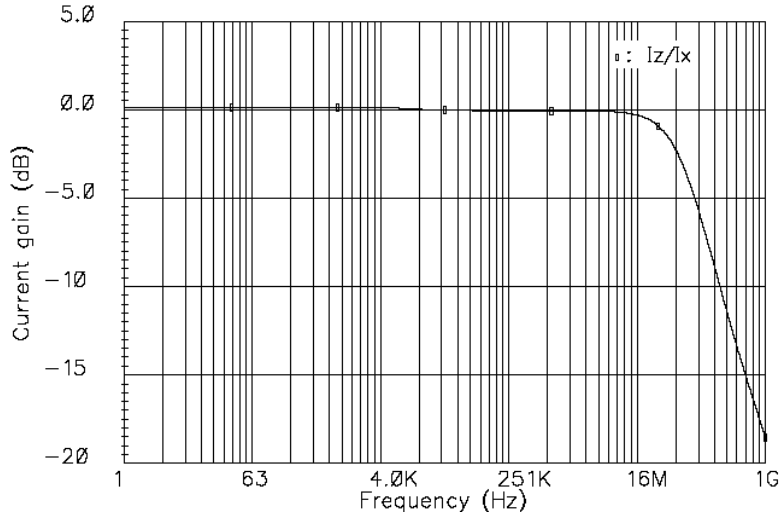


**Fig. 3**: AC analysis of CCII from Fig. 1: Iz/Ix in dB

DC current linearity between X and Z nodes is in interval [-35µA; +35µA] see Fig.4, this range is suitable for many applications, which need low power consumption.

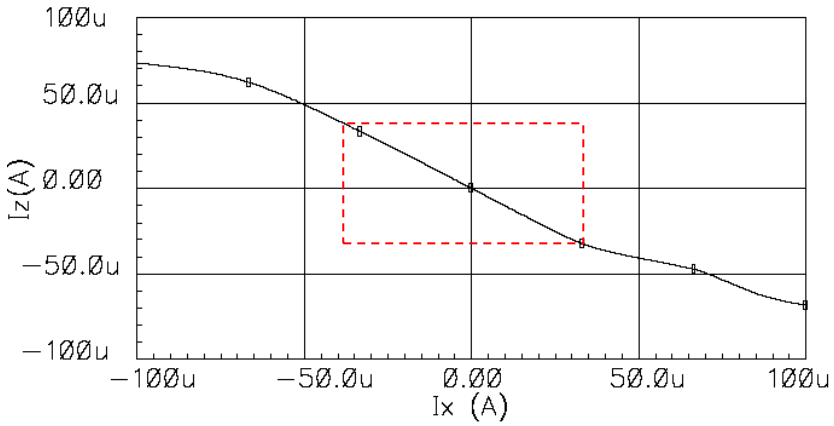


**Fig. 4**: DC analysis of CCII from Fig. 1: Iz versus Ix.

## 3 ACKNOWLEDGMENT

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