Effective Spice Analysis of Switched Capacitor DC-DC Converters

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***Abstract*—An effective Spice analysis of switched capacitor DC-DC converters is proposed. The model of switched circuit is made up in such a way that its transient analysis within a single switching phase results in direct evaluation of the steady-state features such as output voltage ripple, average currents and voltages, powers, and converter efficiency.**

I. INTRODUCTION

Switched converters, based on the technique of switched capacitors (SC), represent an important class of up-to-date circuits for voltage conversion. Their advantage consists in the absence of magnetic devices and thus in the possibility of fully integrated implementation. A brief summary of the main results in SC-converter research and design is given in [1]. Various converter topologies are described in [2]. The paper [3] deals with an important type of DC-DC converters – voltage doublers, based on the principle of charge pump.

Computer analysis of switched converters is traditionally accompanied by a number of problems [5]. The transient analysis in Spice is not appropriate for a case when simulated phenomena consist of a slow transient part and comparatively fast switching effects. In general, such an analysis is time-consuming and usually also affected by cumulative numerical errors. In order to compute important converter characteristics such as output voltage ripple, average values of voltages, currents, and powers, converter efficiency, etc., it is necessary to perform a periodical steady-state analysis with subsequent evaluation of the above quantities. Since the Spice-family programs cannot find the periodical steady state directly, it is necessary to attain it subsequently via tedious and repeated transient analysis.

Conventional LC filter-based switched converters with comparatively large time constants are advantageously modeled by the averaging approach [5], which considerably accelerates the transient analysis via the smoothing of fast switching processes. The averaged waveforms then rapidly converge to the pseudo-DC steady state, which represents the average values of circuit variables in the periodical steady state of converter. These average values then also include information about the average powers and about the converter efficiency.

In contrast to inductor-based switched PWM converters, ideal SC converters are characterized by time constants which are negligible in comparison with the lengths of switching phases. That is why the above averaging techniques cannot be used here. The electric charge, flowing from the outer circuit into the capacitor within the duration of a concrete switching phase, is equal to the product of the capacitance C and the difference of capacitor voltages at the end and the beginning of switching phase. This leads to the formula for equivalent resistance of the switched capacitor $1/(f_sC)$, where f_s is the switching frequency. This formula is well known from the area of SC filters [4]. It can be regarded as a starting point of averaged modeling of SC converters. In reality, the value of equivalent resistance is affected by switch on-resistances as well as ESRs of capacitors [6]. In other words, validity of the above formula is reduced to the area of relatively low time constants in the circuit.

A simple method of obtaining the averaging models of SC converters is described in [7]. However, the simulation results are not precise for circuits with comparatively large time constants. This can cause problems when simulating, for example, the influence of switch on-resistances on the output voltage and efficiency. On the other hand, the averaging technique in [8] works well if the capacitor voltages are piece-wise linear functions of time.

The already mentioned drawback of the averaging approach, that is removing the information about the voltage ripple from the simulation results, must be substituted by a tedious steady-state transient analysis of switched-level model of the converter.

A new method of modeling the SC converters is proposed in the paper, enabling a highly efficient Spice analysis: The transient analysis is run only within a part of the switching period (for example, when the duty ratio is 0.5, the analysis runs only within one half of the switching period). The time-consuming and repeated transient analyses are avoided. If the analysis is terminated, the coordinates of the steady-state are known as well as information about the ripple and average values of circuit variables, including the average powers and converter efficiency. The method will be illustrated on the example of an SC voltage doubler [7].

II. MODELING THE SWITCH CAPACITOR VOLTAGE DOUBLER

The switched capacitor voltage doubler [7] and the switching diagram are shown in Fig. 1. Here, D is the duty ratio, D' is the complementary duty ratio ($D'=1-D$), and $T=1/f_s$ is the switching period. The number near the switch shows the number of the switching phase in which the switch is on. A possible steady-state waveform of capacitor voltage is outlined in Fig. (b). The points O

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and □ on the curve at the time instances of ends of switching phases 1 and 2 are numbered ① and ②. In the following, we will assume the on-resistances of all switches to be nonzero. In other words, the waveforms of capacitor voltages will show no discontinuities.

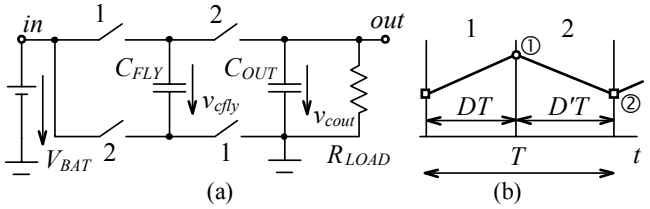

Fig. 1. (a) switched voltage doubler [7], (b) switching diagram.

Due to the linear nature of the converter within each switching phase, its steady-state can be described by the following equations:

End of switching phase 1 – point ①:

$$\begin{bmatrix} v^1_{cfly} \\ v^1_{cout} \end{bmatrix} = \begin{bmatrix} a^1_{11} & a^1_{12} \\ a^1_{21} & a^1_{22} \end{bmatrix} \begin{bmatrix} v^2_{cfly} \\ v^2_{cout} \end{bmatrix} + \begin{bmatrix} b^1_1 \\ b^1_2 \end{bmatrix} V_{BAT} \qquad (1)$$

End of switching phase 2 – point ②:

$$\begin{bmatrix} v^2_{cfly} \\ v^2_{cout} \end{bmatrix} = \begin{bmatrix} a^2_{11} & a^2_{12} \\ a^2_{21} & a^2_{22} \end{bmatrix} \begin{bmatrix} v^1_{cfly} \\ v^1_{cout} \end{bmatrix} + \begin{bmatrix} b^2_1 \\ b^2_2 \end{bmatrix} V_{BAT} \qquad (2)$$

The superscripts of individual voltages denote the number of the switching phase, at the end of which the voltage is read. The „*a*“ and „*b*“ coefficients depend on the nature of transient phenomena in switching phases 1 and 2 as well as on their lengths. For simpler switched circuits, these coefficients can be described by analytical formulae. More advantageously, their numerical values should be evaluated directly by the Spice program.

As is obvious by inspection of Fig. 1 (a), the voltage across capacitor C_{FLY} at the end of phase 1 depends on the battery voltage and on the initial capacitor voltage at the end of phase 2, not on the voltage across C_{OUT} at the end of phase 2. Also, the voltage across C_{OUT} at the end of phase 1 will not depend on the voltage across C_{FLY} at the end of phase 2 and on the battery voltage. Thus

$$a^1_{12} = a^1_{21} = b^1_2 = 0 . \qquad (3)$$

Similar simplifications do not apply in phase 2 because at this phase the circuit topology is not broken into separate parts.

A method for evaluating the „*a*“ and „*b*“ coefficients by means of Spice will be described in Section III. If these coefficients are known, the steady-state capacitor voltages at the ends of switching phases can be directly found by solving the set of equations (1) and (2). The values of these voltages can then serve to compute the output voltage ripple (a difference of voltages across C_{OUT} at the ends of phases 1 and 2) as well as the average values of the input and output currents, output voltage, powers, and efficiency.

During switching phase 1, the following charge flows into the capacitor C_{FLY}:

$$\Delta Q^1_{cfly} = C_{FLY}(v^1_{cfly} - v^2_{cfly}) . \qquad (4)$$

During switching phase 2, the charge will be as follows:

$$\Delta Q^2_{cfly} = C_{FLY}(v^2_{cfly} - v^1_{cfly}) = -\Delta Q^1_{cfly} . \qquad (5)$$

In the steady state, the average capacitor current within one switching period will be zero:

$$\begin{aligned} < i_{cfly} >_T &= < i_{cfly} >_{DT} + < i_{cfly} >_{D'T} = \\ &= \frac{\Delta Q^1_{cfly}}{T} + \frac{\Delta Q^2_{cfly}}{T} = 0 \end{aligned} \qquad (6)$$

However, the partial average currents within phases 1 and 2 are nonzero. Their values can be obtained after substituting (4) and (5) into (6):

$$< i_{cfly} >_{DT} = - < i_{cfly} >_{D'T} = \frac{C_{FLY}}{T}(v^1_{cfly} - v^2_{cfly}) \qquad (7)$$

Similarly, the currents through C_{OUT} are:

$$< i_{cout} >_{DT} = - < i_{cout} >_{D'T} = \frac{C_{OUT}}{T}(v^1_{cout} - v^2_{cout}) \qquad (8)$$

In order to analyze the average quantities in the steady state, capacitors can be substituted by current sources at each switching phase. Their currents are given by the products of equivalent conductivity C/T and the differences between capacitor voltages at the ends of switching phases. The layout is shown in Fig. 2. Note the average values of the current flowing from the battery and of the load current within the total switching period $<i_{in}>_T$ and $<i_{out}>_T$:

$$< i_{in} >_T = 2 < i_{cfly} >_{DT} , \; < i_{out} >_T = < i_{cfly} >_{DT} . \qquad (9)$$

Due to the large capacity of C_{OUT}, the relative ripple of the output voltage will be low, and the average voltage will be proportional to the average load current:

$$< v_{out} >_T = R_{LOAD} < i_{out} >_T \qquad (10)$$

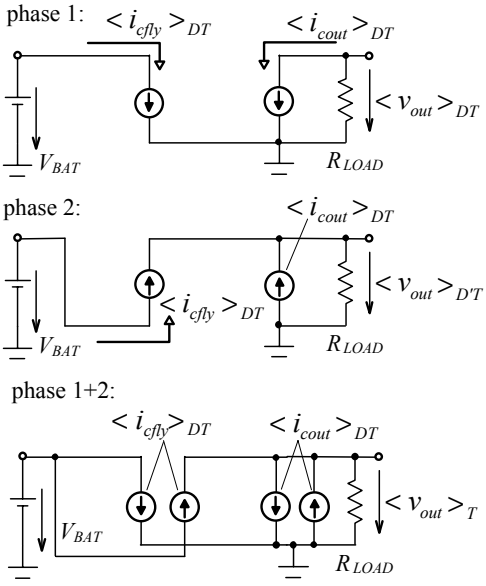

Fig. 2. Layout for computing average values of currents and voltages.

Note that in this model, where capacitors are substituted by current sources, neither the switch on-resistance nor the capacitor ESR affects the input and output currents. That is why they are not included in the schematic.

The average powers and the efficiency can be subsequently determined from the quantities from Eqs. (9) and (10).

III. SPICE IMPLEMENTATION

The Spice implementation is described for the case $D = 0.5$. A modification of the procedure for a general value of duty ratio will be mentioned in the Conclusions.

The „*a*“ and „*b*“ coefficients in Eqs. (1) and (2) can be evaluated via transient analysis within switching phases 1 and 2. The model being analyzed is composed of auxiliary circuits, derived from the converter for the switch states from phases 1 and 2. These circuits can be analyzed simultaneously. When $D = 0.5$, the information given below about the coefficients will be available immediately after terminating the transient analysis at time $T/2$.

It follows from (1) that the coefficients a_{11}^1 and a_{21}^1 are equal to the voltages across C_{FLY} and C_{OUT} at the end of switching phase 1 if C_{FLY} was charged to 1V at the beginning of this phase, if C_{OUT} was discharged, and simultaneously the voltage battery V_{BAT} was zero.

Similarly, the coefficients a_{12}^1 and a_{22}^1 are equal to the voltages across C_{FLY} and C_{OUT} at the end of switching phase 1 if C_{FLY} was discharged at the beginning of this phase, if C_{OUT} was charged to 1V, and simultaneously the voltage battery V_{BAT} was zero.

The coefficients b_1^1 and b_2^1 are equal to the voltages across C_{FLY} and C_{OUT} at the end of the switching phase if both capacitors were discharged at the beginning of this phase, and if the battery voltage was 1V.

Analogous rules are valid for the coefficients from Eq. (2), which can be utilized in Spice by the transient analysis within the auxiliary model of the converter in phase 2.

It is apparent that it is necessary to set up 6 subcircuits for the two-phase SC converter, consisting of 2 capacitors, which are simultaneously analyzed via transient analysis for $T/2$ seconds run. The corresponding capacitor voltages at the end of analysis will be equal to the „*a*“ and „*b*“ coefficients from Eqs. (1) and (2). Another subcircuit provides the solution of these equations aimed at finding the coordinates of the periodical steady state. The coefficients of the equations are modified through the analysis run, but Spice solves the equations continuously. That is why the steady state will be determined correctly just at the end of the analysis run. The last section of the Spice model will compute the average currents and the output voltage from the coordinates of the steady state according to Eqs. (7) – (10). It is useful to evaluate powers and efficiency directly in the Probe postprocessor.

A complete PSpice input file for the simulation of voltage doubler from Fig. 1 (a) is given in Table I. According to [7],

TABLE I. INPUT FILE FOR SC CONVERTER IN FIG. 1 (A)

```
Charge pump - direct steady state analysis
*
.param Cfly 1u C 10u Ron 2 Resr 1 Rload 100
.param Vbat 3V fs 650k d 0.5 d2 {1-d}

X11 0 a111 a211 pump1
.IC V(a111)=1V
X21 0 a121 a221 pump1
.IC V(a221)=1V
X31 in31 b11 b21 pump1
Vbat1 in31 0 {Vbat}
X12 0 a112 a212 pump2
.IC V(a212,a112)=1V
X22 0 a122 a222 pump2
.IC V(a222)=1V V(a122)=1V
X32 in32 b12 b22 pump2
Vbat2 in32 0 {Vbat}

* steady state computation
Ec11 c11 0 value={V(a111)*V(c12)+V(b11)}
Ec21 c21 0 value={V(a221)*V(c22)}
Ec12 c12 0
value={V(a212,a112)*V(c11)+V(a222,a122)*V(c21)+
+V(b22,b12)}
Ec22 c22 0 value={V(a212)*V(c11)+V(a222)*V(c21)+V(b22)}
* end of steady-state computation

* output voltage peak-to-peak ripple
Eripple ripple 0 value={V(c22)-V(c21)}
* averaged input and output current
gIin 0 0 value={2*Cfly*fs*(V(c11)-V(c12))}
gIout 0 outa value={Cfly*fs*(V(c11)-V(c12))}
* averaged output voltage
Routa outa 0 {Rload}
*
.tran 0 769.231n 0 700p skipbp; Tmax=d/fs=769.231ns
.probe

.subckt pump1 in Cfly out
R in Cfly {2*Ron+Resr}
Cfly Cfly 0 {Cfly}
C out 0 {C}
Rload out 0 {Rload}
.ends

.subckt pump2 in Cfly2 out
R in Cfly2 {2*Ron+Resr}
Cfly out Cfly2 {Cfly}
C out 0 {C}
Rload out 0 {Rload}
.ends

.end
```

TABLE II. SWITCH-LEVEL MODEL OF SC CONVERTER IN FIG. 1 (A)

```
Charge pump – switch-level model
*
.param Cfly 1u Cout 10u Ron 2 Resr 1 Rload 100
.param Vbat 3V fs 650k Ts {1/fs} d 0.5 d2 {1-d} T1 {d*Ts}

Vbat 1 0 {Vbat}
Cfly 2 4 {Cfly}
Resr 4 5 {Resr}
Cout 3 0 {Cout}
Rload 3 0 {Rload}
S1 1 2 control 0 Switch
S2 5 0 control 0 Switch
S3 1 5 0 control Switch
S4 2 3 0 control Switch

Vcontrol control 0 PULSE -1 1 0
+ {T1/1000} {T1/1000} {T1-2/1000*T1} {Ts}
.model Switch Vswitch Ron={Ron} Von=0.1V Voff=-0.1V
*
.tran 0 2.5m 0 0.01538u skipbp
.probe

.end
```

identical on-resistances R_{ON} of switches and the ESR of C_{FLY} are included in the model. For the converter parameters from the input file, the average value of output voltage is found to be 4.9983V with a ripple of 3.8448mV, and the computed average values of input and output currents are 99.966mA and 49.983mA, respectively. These values lead to average input and output powers of 299.898mW and 249.83mW, respectively. The resulting converter efficiency is thus 83.305%. The total PSpice job time of the above steady-state analysis is only 0.64s (AMD Athlon™ 64 Processor 2.21 GHz, 2GB RAM).

The results of the Performance analysis, based on the PSpice multiple run while stepping the load resistance, are in Fig. 3.

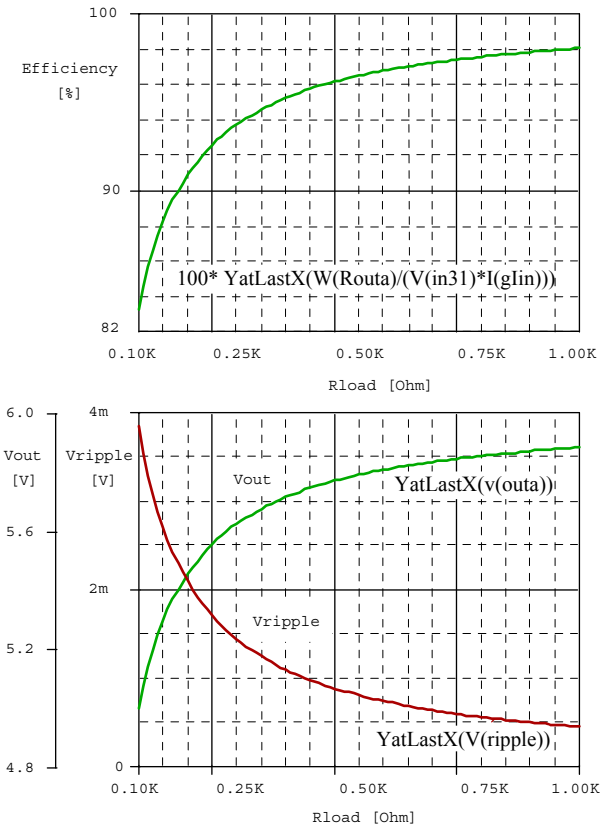

Fig. 3. Results of PSpice simulation: Efficiency, output voltage, and its ripple versus load resistance.

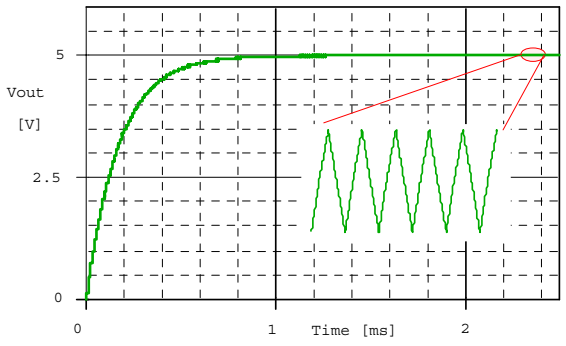

Fig. 4. Results of transient analysis of conventional switched-level model.

The computed values of converter output voltage and its ripple were compared with the outputs of the conventional time-consuming transient analysis. The corresponding PSpice circuit file is given in Table II. In order to provide a reasonable accuracy, the step ceiling of the transient analysis was set to one hundredth of the switching period. The steady state was reached after ca. 2.5ms, i.e. within 1625 switching periods. The analysis ran for 36.23 seconds, i.e. almost 60 times more than for the proposed method. The steady-state output voltage varies between the values 4.9962V and 5.0001V. The corresponding average value and peak-to-peak ripple are 4.99815V and 3.9mV, respectively, which confirms the above results of the proposed direct steady-state computation.

IV. CONCLUSIONS

The method described consists in a special model of SC converter, to which the Spice transient analysis is applied. In contrast to the previous methods, the analysis run is applied only within one half of the switching period. At the end of the analysis, data are available which were previously analyzed via a time-consuming transient analysis of the steady-state of switch-level model of the converter (ripple of the circuit variables) and via the averaging approach (average values of voltages, currents, power, and converter efficiency). The method works well for general values of time constants of circuit transients. A certain drawback consists in the necessity to set up $2(N_C+1)$ partial converter models for automated steady-state computation, where N_C is the number of capacitors in the converter.

In the case of general value of duty ratio, when the switching phases are of different lengths, the transient analysis must be performed within the longer phase. Then the „*a*“ and „*b*“ coefficients for the shorter phase will be determined by means of a simple model of the type of Track-Hold circuits.

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