NONRECURSIVE FILTERS FOR ANALOG SIGNAL PROCESSING

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Abstract

The filter structures with constant group delay for analog signal processing are presented. These filters are based on the discrete-time FIR structures with principally linear phase frequency responses. The block of time delay can be realized either by the Track-Hold circuit or using switched capacitor technique.

Introduction

In general, classical analog filters – both passive and active - have the nonlinear phase frequency response, i.e. the group delay depends on frequency. This phenomenon is principal and we can only partly reduce it in certain frequency band using suitable approximation of the magnitude response.

The discrete and digital filters offer the solution as the well-known filters with the finite impulse responses (FIR). Fulfilling some condition, these filters have exactly linear phase response over all frequency range. Such filters can be realized by the nonrecursive structures as the chain of delay registers. Because the transmission properties of the analog delay element cannot be exactly described as the finite order rational fraction function of the Laplace operator *s*, the nonrecursive filters do not appear as the analog polynomial filters with the lumped parameters. In the classical analog filters, various feedback relations among the circuit variables (both apparent and hidden) always exist. That is why they are nonrecursive filters with the nonlinear phase frequency response.

The FIR filters can be realized using the switched capacitor or other switched techniques. Because the delay block is realized using the switched circuits without problem, we can perform the analog signal processing using the nonrecursive structures. However, in reality we have to overcome serious problems concerning the real properties of the discrete analog switches and of the active elements for the sampling frequencies over 1MHz.

In the contribution, we describe the possible way of the synthesis and circuit realization of switched nonrecursive filters. These filters can be compiled either by the special switched FIR integrated blocks or by some novel fast discrete components of the analog signal processing.

Realization forms of the discrete-time prototype

The discrete-time FIR filter with the constant group delay is the prototype of our design. Two well-known realization forms of FIR filters are in Fig. 1 a and b. The z-domain system function is the same for both structures:

$$K(z) = \sum_{k=0}^{N} a_k z^{-k} \tag{1}$$

where N is the filter order. The coefficients of the system function can be designed from the filter specification in the frequency domain using some of standard procedures. In view of the filter purpose (analog signal filtering), the sampling frequency has to be at least 30-100 times above the pass-band frequencies. However, the maximum sampling frequency is limited by the real properties of the discrete components, especially the analog switches.

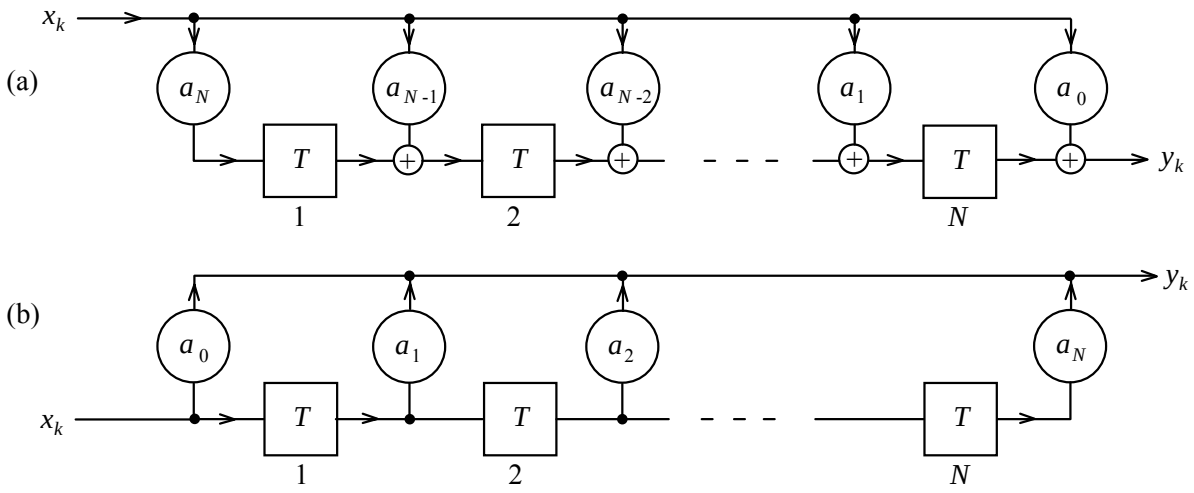

Fig. 1. The first (a) and the second (b) realization form of the FIR discrete-time filter.

There are more possibilities how to realize the delay blocks T ($T = 1/f_S$). One solution is in Fig. 2 that utilizes the Track-Hold (TH) circuits with the inverse sampling signals. The weighting coefficients of the system function can be implemented using the proper resistive net of the operational amplifiers.

As shown below, the first filter structure enables more efficient solution based on the switched capacitor approach.

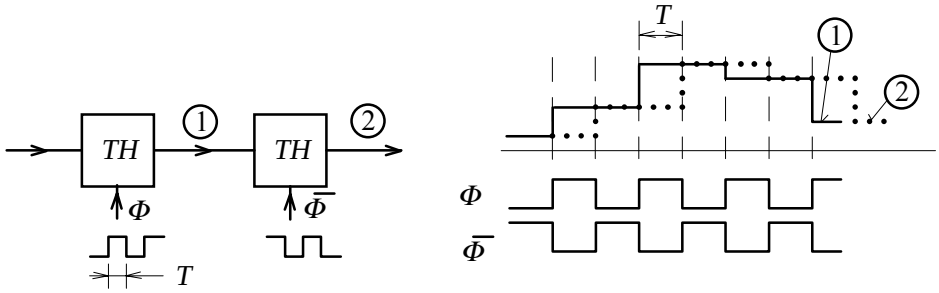

Fig.2. Possible realization of the delay block using the Track-Hold circuits.

Switched building block of the first filter structure

The principle is in Fig.3. The switch near the signal source along with the capacitor C and the unity gain buffer compile the TH circuit. During the switching phase 1, the capacitor C is charged to the voltage v . At the same time, the capacitor a_iC is charged to the voltage x. In the phase 2, the capacitor a_iC is connected between the input and output outlets of the buffer and its charge is completely moved to the capacitor C. After this transfer, the output voltage is the sum according to the Fig. 3. It should be also noted that the negative coefficient of the system function can be simply realized by interchanging of the outlets for charging of the capacitor from the source x.

As shown below, the N-th order filter can be compiled using $5N$ switches, N+1 buffers, $2N$ capacitors and 2 resistors.

In case of filters with the pass-band frequencies round 100kHz, the sampling frequencies from 10MHz are required. For these frequencies, the serious design problems appear. The second problem is the filter complexity: order of the FIR structures is much greater then the order of the feedback structures to achieve comparable magnitude responses. For these

reasons, the discrete realization is expedient only for the lower orders. The only way how to realize high order FIR structures is to use specially developed integrated building blocks.

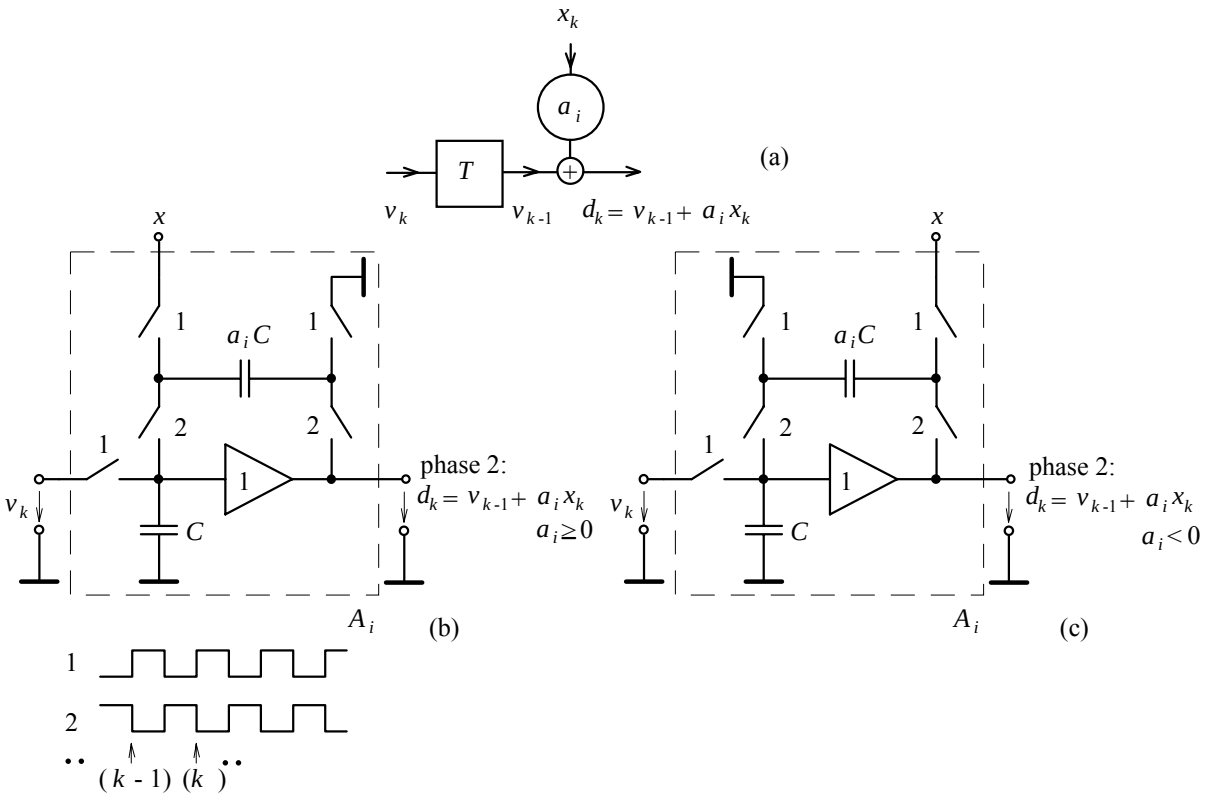

Fig. 3. (a) Part of the filter from the first structure, (b), (c) the switched building block for the positive and the negative coefficient of the system function.

Suitable elements for the discrete realization

Following integrated circuits are suitable for discrete realization:

AD9101 – monolitic sampling amplifier (SH), 125 MHz sampling rate.

AD8182 – dual fast video multiplexers, Turn-On/Turn-Off time 10ns.

LT1205 – cheaper variant of AD8182, Turn-On/Turn-Off time 25ns.

AD8170 – fast multiplexer, Turn-On/Turn-Off time 10ns, internal current feedback amplifier.

ADG201HS – high speed, quad switch, 50ns max t_{ON} and t_{OFF}.

BUF04 – closed-loop high-speed buffer, bandwidth 110MHz, slew rate 3000V/μs, optimized to drive capacitive loads.

For excellent sampling rate, the utilization of sampling amplifier AD9101 represents the best solution. Main disadvantages are the expensive solution and exacting realization of PCB.

The fast TH circuits can be compiled from the multiplexers AD8182, LT1205 or AD8170. However, their internal structure with the isolation buffer in each channel does not allow efficient utilization of the whole integrating circuit for our purposes. To construct whole filter, the additional elements are needed to realize equation (1). The final circuit is then inadequately complicated and expensive.

The reasonable compromise is described solution based on the first realization form with the analog switches ADG201HS and the buffer BUF04. Because the maximum switching frequency does not exceed 10MHz, described conception is suitable for the filters with the frequency range up to hundreds of kHz.

Realization example

Let us consider discrete-time lowpass filter with the sampling frequency 100kHz, flat pass-band response and constant group delay. The cutt-of frequency is 3,4kHz and required attenuation 40dB from the frequency 20kHz. The filter order is $N = 12$ and its coefficients are as follows:

$$a_0 = \ 7{,}52480\text{E-}3 \quad = a_{12}$$
$$a_1 = \ 1{,}72905\text{E-}2 \quad = a_{11}$$
$$a_2 = \ 2{,}99145\text{E-}2 \quad = a_{10}$$
$$a_3 = \ 4{,}36638\text{E-}2 \quad = a_9$$
$$a_4 = \ 5{,}61360\text{E-}2 \quad = a_8$$
$$a_5 = \ 6{,}48632\text{E-}2 \quad = a_7$$
$$a_6 = \ 6{,}80000\text{E-}2 \quad = a_6$$

Resulting scheme is in Fig. 4.

The computer simulation using the program SPIN [3] confirmed the design requirements. Construction and the measurement will be realized after receiving adequate amount of integrated switches and buffers.

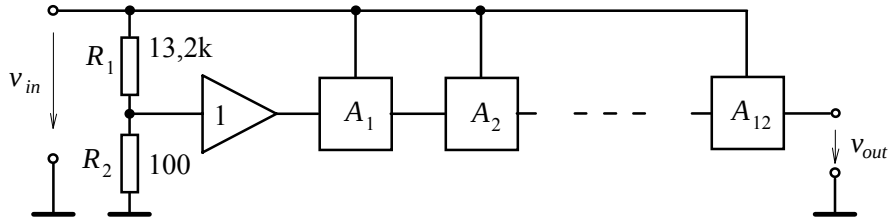

Fig. 4. Designed filter. The structure of blocks A_i is given in Fig. 3 (b).

Conclusion

Novel filter realization with the principally constant group delay is described. This solution is based on the switched capacitor approach. For most applications, the relative high orders of the FIR structures are required. The corresponding circuit then complicated. One perspective solution is to develop such integrated switched blocks which will be completed by additional capacitors to adjust required filter coefficient independently.

References

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[2] Catalogue, Linear Technology, 1997.
[3] BIOLEK,D.: Modeling of Periodically Switched Networks by Mixed s-z Description. IEEE Trans. on CAS-I, Vol. 44, No. 8, August 1997, pp. 750-758.