

ORDER OF Z-DOMAIN MODEL OF SWITCHED CIRCUIT

DALIBOR BIOLEK Viera BIOLKOVÁ*

Dept. of Microelectronics *Radioelectronics

Brno University of Technology

Udolní 53, 602 00 Brno

CZECH REPUBLIC

dalibor.biolek@vabo.cz http://www.vabo.cz/stranky/biolek

Abstract - A method of identifying the order of the switched circuit as a z-domain dynamic system is described. The method is readily algorithmized and it can be implemented into current analyzing programs to avoid zeros and poles, which appear due to numerical inaccuracies.

Key-Words: - switched circuit, system function, z-domain order

1 Introduction

The terms *state*, *state variables*, and *system order* are familiar from the classical theory of linear systems. For an electrical circuit, the order cannot exceed the number of circuit storage elements. There are exact rules how to find its true size.

The above rules are important not only for theoretical analyses. For example, algorithms of computer semisymbolic analysis of large systems or finding zeros and poles of circuit functions represent a sophisticated numerical task. Knowing the resulting order in advance, we can avoid false solutions due to numerical inaccuracies.

For switched circuits, especially for circuits comprising analog periodically controlled switches, no rules for finding the circuit order have been published till now. Switched capacitor and switched current circuit are typical representatives of such circuits. The discrete-time character of their operation is modeled by z-domain poles of the corresponding circuit functions [1]. As shown in the paper, the order of such systems depends – surprisingly enough – on several factors, for instance on parasitic R_{on} resistances of switches. One possible method how to solve this problem for systems with two-phase switching is proposed.

2 Opening example

Consider the two-phase switched circuit in Fig. 1. The numbers above the individual switches indicate the phases in which the switches are in “ON” state.

The circuit was analyzed by the SPIN program [1] to find its z-domain poles. For the analysis, all the combinations of zero- and nonzero R_{on} switches were considered. The results are summarized in Table 1.

S_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
S_3	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
order	2	2	2	3	2	3	2	3	2	3	2	3	3	4	3	4

Tab. 1. Dependence of the order of the circuit in Fig. 1 on whether switch resistance R_{on} is zero (0) or not (1).

The zeros and ones in rows “S” represent the zero- and non-zero R_{on} resistance of the corresponding switch. For simplicity, let the zero/non-zero R_{on} switch be called ideal/non-ideal switch, respectively. It should be noted that the circuit order changes between the values 2 and 4, depending on the combination of ideal/nonideal switches in the circuit.

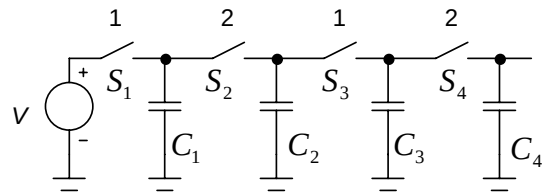


Fig. 1. Example of circuit with two-phase switching.

Let us consider the circuit order as a real function of Boolean variables S_1 , S_2 , S_3 , and S_4 . An analysis of Table 1 yields the following conclusions:

- The order does not depend on switch S_3 .
- The order is 2 if switch S_4 is ideal and if at least one of switches S_1 and S_2 is ideal.
- The order is 3 if switch S_4 is non-ideal and if at least one of switches S_1 and S_2 is ideal, or if switch S_4 is ideal and both switches S_1 and S_2 are non-ideal.
- The order is 4 if all switches S_1 , S_2 and S_4 are non-ideal.

The above example can evoke the following general questions concerning the circuits with external switching:

- What are the theoretical boundaries within which the order can vary in dependence on the parameters of the individual circuit elements, when the number of storage elements is known?
- Does any simple rule exist how to establish the order of a concrete circuit?

A possible way of finding the answers will be described below.

3 Circuit analysis in the light of memory effects

The order of switched circuit will depend on how the individual storage elements will behave as memory elements both during the switching phases and in the transitions between the phases. We will show that the upper boundary of order is given by the number of storage elements, and the lower boundary will depend on the topology of switched circuit.

The special graph in Fig. 2 (a) describes memory effects in the circuit in Fig. 1 during the transition from phase 1 to phase 2. For example, it is obvious that the voltage across capacitor C_1 in phase 2, when capacitors C_1 and C_2 are interconnected by switch S_2 , will depend both on the voltage across C_1 in the previous phase and on the voltage across C_2 in the previous phase. This dependence is modeled in the graph by two paths which are directed from the level „phase 1“ to the „phase 2“ level. To find the circuit order, it is not necessary to assign gains to each path. We must only take into account that - in the z -domain - every transition between any given levels is accomplished by the multiplying factor $z^{-1/2}$.

Fig. 2 (b) illustrates the back transition from phase 2 to phase 1. It should be noted that closed loops have appeared in the graph within the frame of nodes V_C – voltage across individual capacitors in both phases, and so have closed loops between voltage nodes of different capacitors. The gain of the first mentioned loops is characterized by the multiplying factor z^{-1} . Because these four loops do not touch one another, the resulting circuit order is according to the Mason's gain formula [2,3,4] 4.

Fig. 3 models the case when all the switches are ideal. Then in phase 1, C_2 and C_3 are in parallel, and so are the couples C_1 - C_2 and C_3 - C_4 in phase 2. This results in the equality of the corresponding voltages and in the reduction of state variables in the given switching phase. This fact is modeled in the graph by the joining line between the corresponding voltage nodes. Moreover, capacitor C_1 does not operate as memory element in phase 1 due to the influence of ideal switch S_1 (C_1 is

connected to voltage source). That is why the path from phase 2 to phase 1 is omitted in the graph. It is obvious from Fig. 3 that the circuit order is now 2 (only 2 non-touching loops are in the graph, i.e. the loops of nodes v_{C2} and v_{C4}).

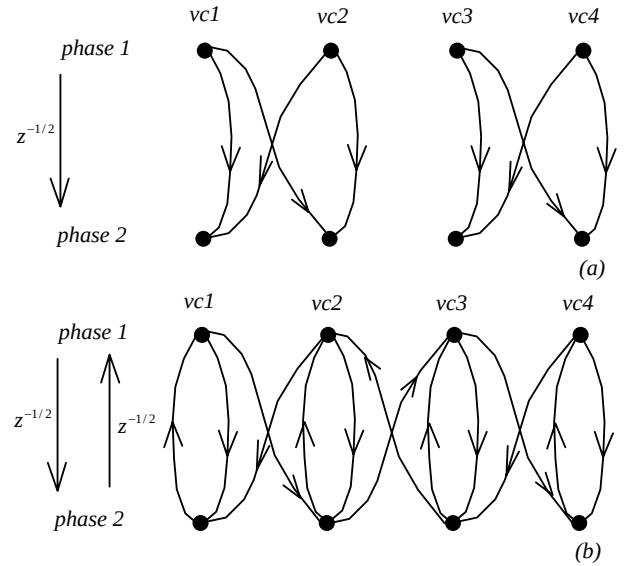


Fig. 2. Graph describing the memory effects in the circuit for non-ideal switches, for transitions (a) from phase 1 to phase 2, (b) among phases 1-2-1.

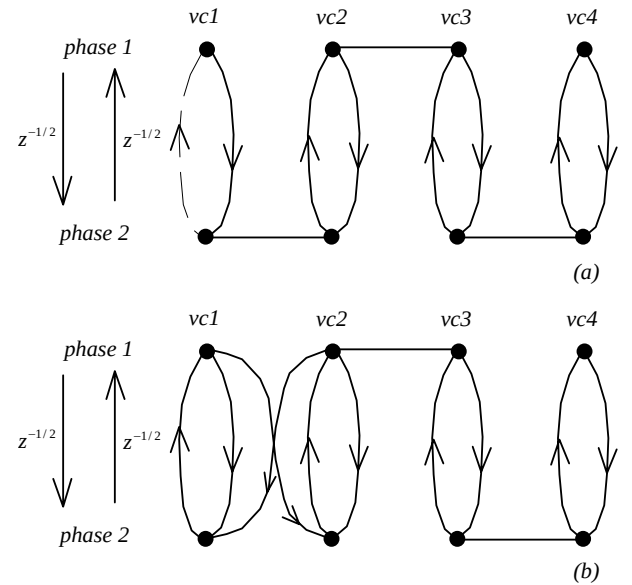


Fig. 3. Graph for (a) ideal switches, (b) non-ideal switches S_1 and S_2 and ideal switches S_3 and S_4 .

Some more conclusions can be drawn from the graph. If during the charging of C_1 from the input port in phase 1 the transient phenomena cannot be neglected, it will not increase the order on the assumption of ideal switches S_2 to S_4 : though, the graph will be completed by the dashed path, order 2 will not be increased. Only the combination with non-zero R_{on} of switch S_2 will change the order (see

Fig. 3b): now capacitors C_1 and C_2 will not be in parallel in phase 2, and they will behave as two independent memory elements. Then it is necessary to remove the joining line between nodes v_{c1} and v_{c2} in phase 2. Three non-touching loops will appear in the graph and the circuit order will be increased to 3.

4 Generalization

With regard to the above analysis, we can draw the following conclusions.

The circuit order is affected by two factors:

- (1) By the number of independent state variables in each switching phase.
- (2) By the manner in which each storage element behaves in the frame of one closed switching cycle, concretely, whether the state of this element depends on its state in the foregoing cycle.

The concrete algorithm of finding the circuit order is as follows:

- (1) We draw the voltage nodes in the graph. We model the prospective dependence of state variables by the joining lines.
- (2) We plot the appropriate paths that model memory effects between switching phases.
- (3) The circuit order is given by the number of mutually non-touching loops in the graph.

5 Conclusion

This paper presents a simple method how to find the z-domain order of two-phase switched networks. The method described can easily be extended to the case of circuits with general n -phase switching. The algorithm has been applied to the SPIN software tool for semisymbolic analysis of circuits with external switching [1].

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