SFG Simulation of General Ladder Filters Using CDBAs

Dalibor Biolek* Viera Biolková**

Abstract **- Simulation of passive ladder LC filters by active circuits with CDBA (Current-Differencing Buffered Amplifier) elements is presented. The so-called "VIV" flow graphs are introduced as a supporting tool of the synthesis of leapfrog active filter and for its subsequent optimization.**

1 INTRODUCTION

The CDBA (Current-Differencing Buffered Amplifier) circuit element, introduced in [1], is a special type of generalized voltage conveyor [2]. It is particularly appropriate for the synthesis of voltage-mode active filters because it enables easy realization of inverting and non-inverting multiple-input integrators.

A leapfrog simulation of classical ladder low-pass and bandpass filters without transmission zeros using the CDBAs is described in [3]. Obviously, this approach can also be applied to other ladder structures. However, the resulting active filter will differ from the passive prototype in some features. It is necessary to analyze, for instance, the dynamic range, the spread of the *R* and *C* values, and the sensitivities.

This paper is organized as follows: In Section 2 we introduce so-called "VIV" flow graphs for efficient description of circuits containing the CDBA elements. These graphs will be used in the synthesis and optimization of active filter. In Section 3 we then explain the composition of a filter "VIV" graph from the familiar voltage and current equations of the ladder filter, as well as the leapfrog CDBA-based filter synthesis from the "VIV" graph. Section 4 shows two propositions, which result from the graph description, helping us to optimize the active filter. The final Section 5 demonstrates the optimization of dynamic range and setting the current gain of a 10MHz bandpass filter.

2 CDBA AND ITS DESCRIPTION BY THE "VIV" FLOW GRAPHS

The behavioral model of ideal CDBA is shown in Fig. 1. This element has two difference current inputs *p* and *n*. The difference of these currents flows from terminal *z* into an outside load. The voltage across the *z* terminal is transferred to the *w* terminal by a unity-gain buffer.

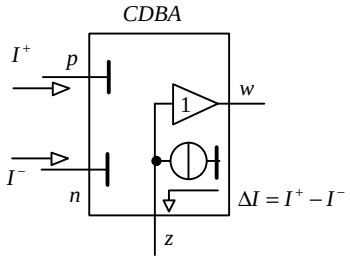

Figure 1: Behavioral model of CDBA element.

The basic CDBA connection is given in Fig. 2 (a), where currents flow into the *p* and *n* terminals from voltage sources through general impedances. The difference current flows from the *z* terminal into an impedance *Z* and generates the voltage

$$V_z = Z\left(\sum_{i=1}^{m} Y_i^+ V_i^+ - \sum_{j=1}^{n} Y_j^- V_j^-\right), \qquad (1)$$

which can be taken from the low-impedance *w* terminal. Symbols *Y* denote admittances which correspond to individual impedances *Z*.

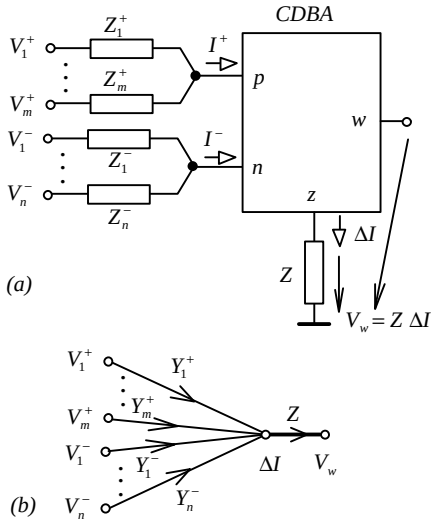

Figure 2: (a) Basic connection of CDBA element, (b) corresponding signal flow graph.

* Department of Electrical Engineering, Military Academy Brno, Kounicova 65, 612 00 Brno, Czech Republic, e-mail: dalibor.biolek@vabo.cz, tel.: +420 541182487, fax: +420 541182888.

** Department of Radioelectronics, Brno University of Technology, Purkynova 118, 612 00 Brno, Czech Republic, e-mail: biolkova@feec.vutbr.cz, tel.: +420 541149152, fax: +420 541149192.

Equation (1) is expressed in the form of simple signal flow graphs (SFG) in Fig. 2 (b). These are so-called „VIV“ (Voltage-Current-Voltage) graphs, originally introduced in [4] for the analysis of *OpAmp* circuits. Note that admittances serve as input voltage/current converters, whereas impedance *Z* is a difference current/voltage converter. When impedance *Z* is realized by a capacitor, then the circuit is a multiple-input universal integrator.

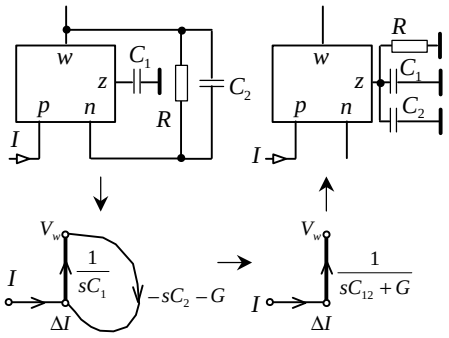

Figure 3: Equivalent circuits with CDBAs and their „VIV“-graphs. Symbol C_{12} is abbreviation of C_1+C_2.

A demonstration of the utilization of „VIV“ graphs is in Fig. 3. Applying the basic flow-graph operation, the “VIV” graph of the left-side circuit can be transferred to the right-side graph. In the corresponding circuit we can both reduce the number of capacitors and convert the floating components into the grounded ones.

3 SFG SIMULATION OF GENERAL LADDER FILTER BY LEAPFROG STRUCTURE USING CDBAs

Consider the ladder filter in Fig. 4. This current-mode sixth-order Chebyshev bandpass filter, designed by the NAFID program [5], has 10MHz central frequency, 1.4MHz bandwidth and 0.1dB passband ripple. The component values are as follows:

R_1=R_2=1kΩ, C_1 = C_5 = 148pF, C_2 = C_4 = 15.9pF, C_3 = 150pF, L_1 = L_3 = 1.55μH, L_2 = 1.39μH.

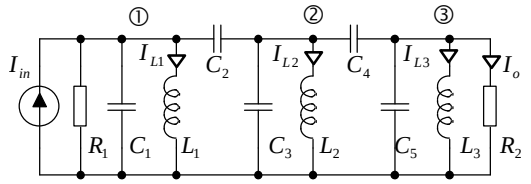

Figure 4: Current-mode sixth-order bandpass filter with coupled LC circuits.

The following equations for voltages and currents can be compiled as a basis of SFG simulation by means of integrating cells [6]:

$$V_1 = \frac{1}{sC_1}[I_{in} - grI_{L1} + sC_2(V_2 - V_1) - G_1V_1],$$

$$rI_{L_1} = \frac{gV_1}{sL_1/r^2},$$

$$V_2 = \frac{1}{sC_3}[sC_2(V_1 - V_2) - grI_{L2} - sC_4(V_2 - V_3)],$$

$$rI_{L2} = \frac{gV_2}{sL_2/r^2} \qquad (2)$$

$$V_3 = \frac{1}{sC_5}[sC_4(V_2 - V_3) - grI_{L3} - G_2V_3],$$

$$rI_{L3} = \frac{gV_3}{sL_3/r^2}.$$

The symbols *r* and *g*=1/*r* denote auxiliary resistances and conductances, respectively, which convert currents into voltages for active SFG simulation. As shown below, these voltages will be realized as *w*-terminal voltages of individual CDBAs.

Equations are expressed by the SFG in Fig. 5 (a). The synthesis of the active filter using CDBAs can be directly performed from this SFG. However, it is useful to first simplify the SFG in the sense of Fig. 3, i.e. to convert the floating impedances between the *w* and *n* terminals into grounded impedances. The modified SFG is in Fig. 5 (b). The corresponding active filter is in Fig. 6.

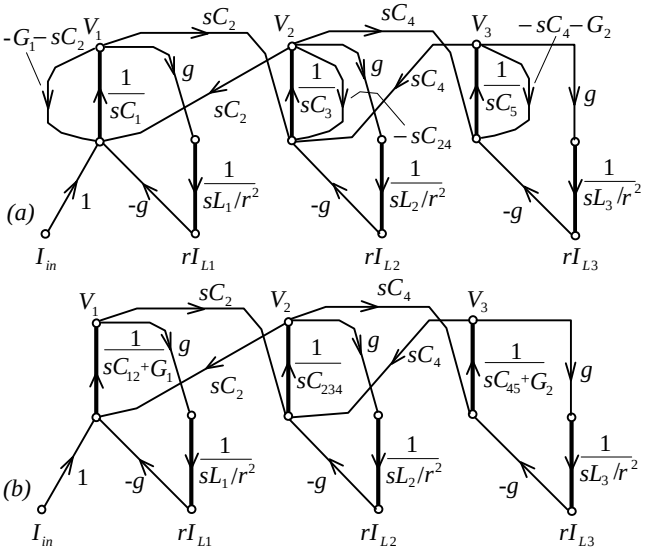

Figure 5: (a) SFG, accordant with equations (2), (b) modified SFG.

Choosing in the first design stage the auxiliary resistance to be *r*=500Ω, we get the component values of designed filter as summarized in Tab. 2, column (a).

The following optimization will –among others- start from the real properties of employed CDBAs. It

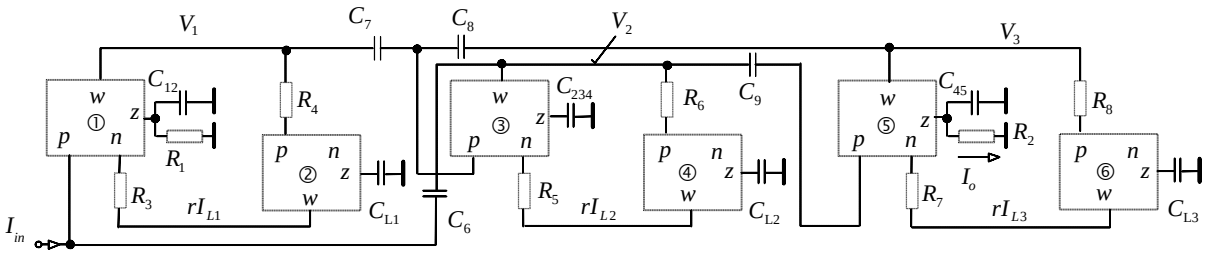

Figure 6: Active filter which corresponds to SFG in Fig. 5 (b).

is necessary to choose the impedance levels with respect to the maximum acceptable currents and parasitic capacitances. The CDBA- based leapfrog structure yields several degrees of freedom, which can be used to optimize dynamic range, spread of component values, etc.

4 PROPOSITIONS WHICH FACILITATE OPTIMIZATION OF CDBA-BASED LEAPFROG STRUCTURES

The following propositions can be derived from the SFG in Fig. 5 (b) or directly from the schematic in Fig. 6. Similar propositions have been conceived earlier [7], [8] for switched-capacitor filters and for continuous-time filters containing grounded *OpAmps* [4].

Proposition 1:

The transfer function from the input to voltage output w of a given CDBA will be increased a-times without affecting the transfer functions from the input into the outputs of the other CDBAs as follows:

We increase *a*-times the impedances of all components that are connected to the *w* and *z* terminals of a given CDBA.

This proposition can be utilized to set the required gain level and to optimize the dynamic range of the filter.

Proposition 2:

The impedance level "around" a given CDBA will be increased a-times without affecting arbitrary node voltage as follows:

We increase *a*-times the impedances of all components that are connected to the *z, p,* and *n* terminals of a given CDBA.

This proposition can be used to set optimum impedance levels and to optimize the spread of *R* and *C* values.

5 OPTIMIZATION EXAMPLE

The optimization procedure will be explained on the preliminarily designed filter in Fig. 6. The CDBAs will be considered within the model published in [9]. This SPICE model of bipolar structure has been designed for the GBW of hundreds of MHz. The outlet currents can be up to 30mA (terminals *p*, *n*, and *z*) or up to 50mA (terminal *w*).

A checking computer simulation of CDBA output voltages of filter in Fig. 6 leads to the curves in Fig. 7. Curve No. 5 confirms the required bandpass response but it is necessary to optimize the upper bound of the dynamic range. The acquired transfer maxima are listed in Table 1. In the column "mult. factor *a*" it is given how many times this transfer must be increased to equalize all the maxima to the level of 0dB.

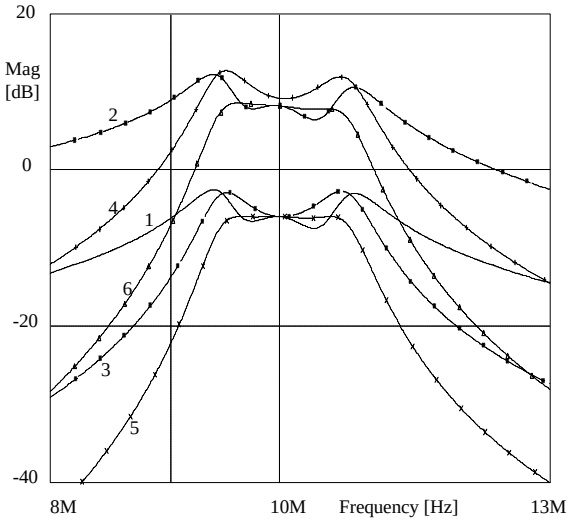

Figure 7: Simulated frequency responses of voltages across *w* – terminals of CDBAs Nos. 1 to 6 in Fig. 6 for 1mA magnitude of the input current.

w output of CDBA No.	max [dB]	mult. factor *a*
1	-2.569	1.344
2	12.199	1/4.073
3	-2.735	1.370
4	12.677	1/4.304
5	-6.023	2
6	8.526	1/2.669

Table 1: Transfer maxima across the outputs of individual CDBAs in Fig. 7.

To equalize the transfer maxima, let us use Proposition 1. For example, modifying the transfer of CDBA No 1 will require multiplying resistances R_1 and R_4 and dividing capacitances C_{12} and C_7 by 1.344. The modified values of all resistances and capacitances are listed in Table 2, column (b). The checking computer simulation has confirmed the required equalization of the maxima.

However, the current transfer I_o/I_{in} is still 1/2. To set the value to 1 without affecting the valid voltage levels, we use Proposition 2: resistances R_2 and R_7 will be decreased two times and simultaneously we double capacitances C_{45} and C_9. The final component values are summarized in column (c) in Tab. 2.

	(a)	*(b)*	*(c)*
R_1	1000	**1344**	1344
R_2	1000	**2000**	**1000**
R_3	500	**122.8**	122.8
R_4	500	**672**	672
R_5	500	**116.2**	116.2
R_6	500	**685**	685
R_7	500	**187.3**	**93.7**
R_8	500	**1000**	1000
C_{12}	163.9	**121.9**	121.9
C_{234}	181.8	**132.7**	132.7
C_{45}	163.9	**82**	**163.9**
C_{L1}	6.2	**25.3**	25.3
C_{L2}	5.56	**23.9**	23.9
C_{L3}	6.2	**16.5**	16.5
C_6	15.9	**11.6**	11.6
C_7	15.9	**11.8**	11.8
C_8	15.9	**8**	8
C_9	15.9	**11.6**	**23.2**

Table 2: Component values of filter in Fig 6. (a) initial, (b) after dynamic range optimization, (c) after setting the current passband gain to 1. All the resistances/capacitances are in ohms/picofarads, respectively.

Finally, a computer simulation of current relations has proved that the maximum outlet currents of CDBAs do not exceed the value of 11mA for the 1mA input current. When appropriate, the optimization via Propositions 1 and 2 is possible, taking into account also the current dynamic range.

6 CONCLUSIONS

Due to the easy implementation of multiple-input integrator, the CDBA element will find application in the synthesis of various forms of active filters. In the case of ladder filter simulation, the circuit topologies containing CDBAs offer more degrees of freedom, which can be used for optimization. The "VIV"-based procedures described in the paper enable the synthesis of general ladder filters and their subsequent optimization.

Acknowledgments

This work is supported by the Grant Agency of the Czech Republic under grants No. 102/01/0432 and No. 102/03/1181, and by the research programmes of BUT MSM 262200022 & MSM 262200011.

References

[1] C. Acar, S. Õzoguz, "A New Versatile Building Block: Current Differencing Buffered Amplifier", Microelectronics Journal 30 (1999), pp. 157-160.

[2] J. Cajka, K. Vrba, "Conveyors – novel active device", Conference STO-8, MA Brno, Czech Republic, pp. 26-29, 2002.

[3] W. Tangsrirat, et al, "Current-Mode Leapfrog Ladder Filters Using CDBAs", Proc. ISCAS'02, Scottsdale (Arizona), May 2002, pp. V-57-V-60.

[4] D. Biolek, V. Biolková, "Modelling and Optimization of Active Filters by Hybrid "VIV-MMC"-graphs", Systems and Control: Theory and Applications, World Scientific, Electrical and Computer Engineering Series, 2000, pp. 381-386.

Electronic file available at

http://www.vabo.cz/stranky/biolek/veda/articles/CSCC00_1.pdf

[5] K. Hájek, J. Sedlácek, "The synthesis with internal optimization loops and internal analysis", International AMSE conference SYS 94, Lyon 1994, pp.263-266.

[6] R. Schaumann, M. S. Ghausi, K. R. Laker, "Design of Analog Filters", Prentice Hall, 1990.

[7] R. Gregorian, K. Martin, G. Temes, "Switched Capacitor Circuit Design", Proc. IEEE, 1983, pp. 941-956.

[8] R. Gregorian, G. Temes, "Analog MOS Integrated Circuits for Signal Processing", John Willey&Sons, 1986.

[9] I. Lattenberg, K. Vrba, "Immittance Inverter with Voltage Conveyors for Analog Signal Processing", Internet Journal

ElectronicsLetters.com, Paper: # 11/11/2002.

Electronic file available at

http://www.electronicsletters.com/papers/2002/0025/paper.asp